MPQ7928

MPSafe™ QM, 18V, 4-Channel PMIC with 3 Bucks and 1 LDO, AEC-Q100 Qualified

DESCRIPTION

The MPQ7928 is a power management solution which integrates three high-efficiency step-down DC/DC converters and a low-noise low-dropout (LDO) regulator. The unique, dual-stage, 18V buck architecture maximizes efficiency for the 1.8V image sensor I/O rail in the CMOS sensor found in high-resolution camera modules.

Constant-on-time (COT) control with phase-locked loop (PLL) provides a fast transient response time. The 2.2MHz fixed switching frequency (f_{SW}) during continuous conduction mode (CCM) mode greatly reduces external inductor and capacitor sizes.

The I²C digital interface allows for application flexibility. The output voltage (V_{OUT}), power sequence, and protection thresholds can all be adjusted through the interface. Fault statuses can also be monitored. Protection features include under-voltage lockout (UVLO), over current protection (OCP), over voltage protection (OVP), under voltage protection (UVP), and thermal shutdown (TSD).

The MPQ7928 minimizes the need for a number of external components and is available in a space-saving QFN-15 (2.5mmx3.5mm) package with wettable flanks. It is available in AEC-Q100 Grade 1.

FEATURES

- Optimized for Automotive Cameras
  - Buck 1: 600mA with 3.5V to 18V Input Voltage (V_{IN})
  - Buck 2: 600mA with 3.5V to 18V V_{IN}
  - Buck 3: 1A with 2.5V to 4V V_{IN}
  - LDO: 200mA for Large CMOS Sensors
- Optimized for EMC/EMI
  - 2.2MHz Fixed Switching Frequency (f_{SW})
  - Spread Spectrum with On/Off Function
  - Symmetric Input Capacitor for Better EMI
  - CISPR25 Class 5 Compliant
  - MeshConnect™ Flip-Chip Package
- Additional Features
  - Selectable Discontinuous Conduction Mode (DCM) and Forced Continuous Conduction Mode (FCCM)
  - Over-Current Protection (OCP) with Valley-Current Detection and Hiccup Mode
  - Power Good (PG)Output
  - I²C Compatible Interface with Packet Error Checking (PEC)
  - Available in a QFN-15 (2.5mmx3.5mm) Package
  - Available with Wettable Flanks
  - Available in AEC-Q100 Grade 1
- Functional Safety System Design Capable:
  - MPSafe™ QM Documentation Available

MPSafe™ QM

APPLICATIONS

- Automotive Camera Modules
- Automotive Sensor Applications
- Automotive Secondary Regulation
- Space-Constrained Applications

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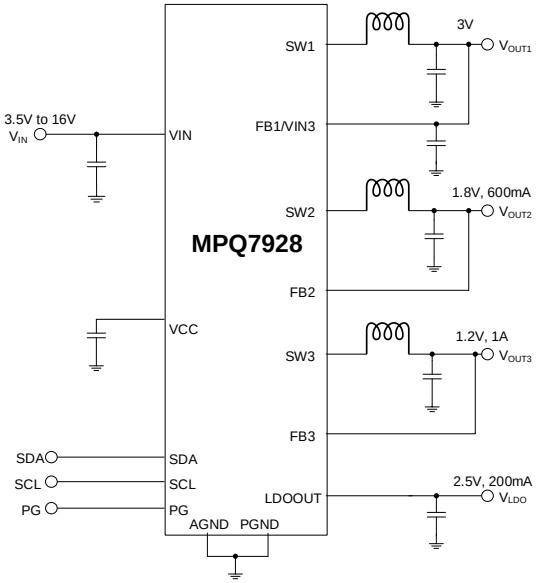
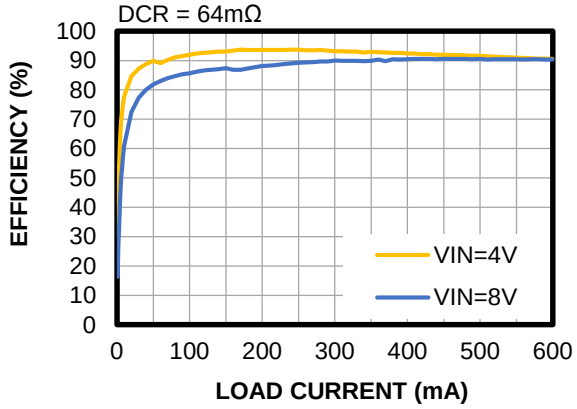
TYPICAL APPLICATION



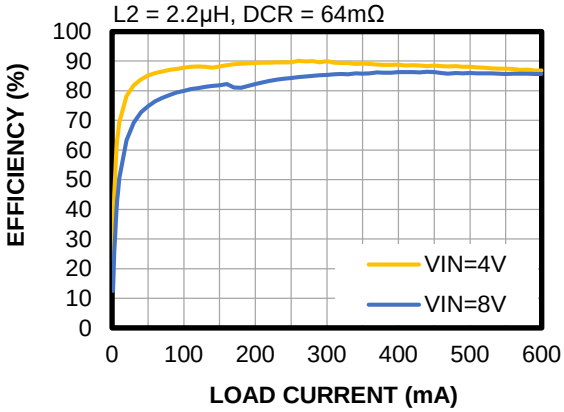
Efficiency vs. Load Current (Buck 1)

V_{OUT1} = 3V, f_{SW1} = 2.2MHz, DCM, other channels are disabled, L1 = 2.2µH, DCR = 64mΩ



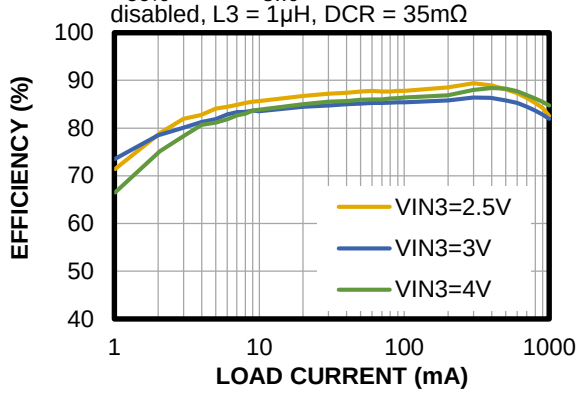
Efficiency vs. Load Current (Buck 2)

V_{OUT2} = 1.8V, f_{SW2} = 2.2MHz, DCM, other channels are disabled, L2 = 2.2µH, DCR = 64mΩ



Efficiency vs. Load Current (Buck 3)

V_{OUT3} = 1.2V, f_{SW3} = 2.2MHz, DCM, LDO is disabled, L3 = 1µH, DCR = 35mΩ



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ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating****
MPQ7928GRHE-xxxx-AEC1**, ***	QFN-15 (2.5mmx3.5mm)	*See Below*	1

* For Tape & Reel, add suffix -Z (e.g. MPQ7928GRHE-xxxx-AEC1-Z).

** "xxxx" is the configuration code identifier for the register settings stored in the OTP register. The default code is "0000". Contact an MPS FAE to create this unique number.

*** Wettable Flanks

**** Moisture Sensitivity Level Rating

TOP MARKING

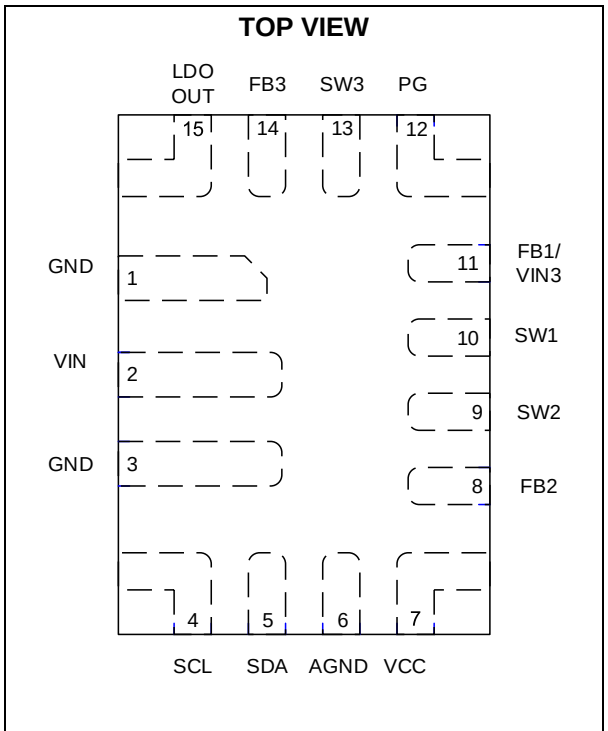
BQP

YWW

LLL

BQP: Production code of MPQ7928
Y: Year code
WW: Week code
LLL: Lot number

PACKAGE REFERENCE



QFN-15 (2.5mmx3.5mm)

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PIN FUNCTIONS

Pin #	Name	Description
1, 3	GND	**Power ground.** The two GND pins are connected inside. These pins should be electrically connected to the system power ground plane with the shortest and lowest-impedance connection possible.
2	VIN	**Input supply voltage.** VIN supplies power to all the internal control circuitry and the power switch connected to SW1 and SW2. To minimize switching spikes, place a decoupling capacitor from VIN to ground, and close to VIN.
4	SCL	**I²C clock pin.** Use an external pull-up resistor to connect the SCL pin to the external I²C supply rail. Connect SCL to ground if it is not used.
5	SDA	**I²C data pin.** Use an external pull-up resistor to connect the SDA pin to the external I²C supply rail. Connect SDA to ground if it is not used.
6	AGND	**Analog ground.** AGND is the reference ground for the internal logic and signal circuit. AGND is internally connected to GND. AGND should be connected to GND in the PCB layout design.
7	VCC	**Biased supply.** The VCC pin supplies power to the internal control circuit and gate drivers. VCC is typically 5V. A decoupling capacitor (recommended to be 4.7µF) connected from VCC to ground should be placed close to this pin.
8	FB2	**Feedback for buck 2.** Connect the FB2 pin directly to buck converter 2's (buck 2) output. See the VOUT_COMMAND (21h) section on page 49 for the V_{OUT2} setting.
9	SW2	**Buck 2 switch node.** The SW2 pin is the output of the internal power switch. Connect SW2 to an external inductor using a wide PCB trace.
10	SW1	**Buck 1 switch node.** The SW1 pin is the output of the internal power switch. Connect SW1 to an external inductor using a wide PCB trace.
11	FB1/VIN3	**Feedback for buck 1 and power source for buck 3 and the LDO.** Directly connect the FB1/VIN3 pin to buck converter 1's (buck 1) output. See the VOUT_COMMAND (21h) section on page 42 for the V_{OUT1} setting. To minimize switching spikes, place a decoupling capacitor from FB1/VIN3 to ground, and placed as close as possible to FB1/VIN3.
12	PG	**Power good output.** The output of the PG pin is push-pull. The high output level can be configured to either 3.3V or 1.8V. Float the PG pin if it is not used.
13	SW3	**Buck 3 switch node.** The SW3 pin is the output of the internal power switch. Connect SW3 to an external inductor using a wide PCB trace.
14	FB3	**Feedback for buck 3.** Directly connect the FB3 pin to buck converter 3's (buck 3) output. See the VOUT_COMMAND (21h) section on page 52 for the V_{OUT3} setting.
15	LDOOUT	**LDO output pin.** See the VOUT_COMMAND (21h) section on page 62 for the V_{LDO} setting. A 2.2µF ceramic capacitor is recommended for the LDO output.

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ABSOLUTE MAXIMUM RATINGS (1)

V_{VIN}……-0.3V to +21V
$V_{SW1/2}$……..0.6V (-5V for <10ns) to V_{IN} + 0.3V
All other pins…… -0.3V to +6.25V
Continuous power dissipation (T_A = 25°C) (2)(6)
QFN-15 (2.5mmx3.5mm)…… 5.95W
Junction temperature (T_J) .....150°C
Lead temperature…….... ……...260°C
Storage temperature……..... -40°C to +150°C

ESD Ratings

Human body model (HBM).....Class 2 (3)
Charged-device model (CDM).....Class C2b (4)

Recommended Operating Conditions

Supply voltage (V_{IN})…… 3.5V to 18V
Buck 1 output voltage (V_{OUT1}).....2.5V to 4V
Buck 2 output voltage (V_{OUT2}).....0.6V to 3.75V
Buck 3 output voltage (V_{OUT3}).....0.6V to 2.55V
LDO output voltage (V_{LDO}).....0.6V to 3.75V
Operating junction temp (T_J).... -40°C to +150°C

Thermal Resistance θ_{JA} θ_{JC}

QFN-15 (2.5mmx3.5mm)
JESD51-7.....…….....51…...5...°C/W (5)
EVQ7928-RH-00A.....……..21…..1.7..°C/W (6)

Notes:

1) Exceeding these ratings may damage the device. Absolute maximum ratings are rated under room temperature, unless otherwise noted. Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can cause excessive die temperature, and the regulator may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) Per AEC-Q100-002.
4) Per AEC-Q100-011.
5) Measured on a JESD51-7, 4-layer PCB. The values given in this table are only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application. The value of θ_{JC} shows the thermal resistance from junction-to-case bottom.
6) Measured on MPS's standard evaluation board for the MPQ7928: a 6.35cmx6.35cm, 2oz copper, 4-layer PCB. The value of θ_{JC} shows the thermal resistance from junction-to-case top.

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ELECTRICAL CHARACTERISTICS

V_{IN} = 8V, T_J = -40°C to +150°C, typical values are at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input Voltage (V_{IN}) Supply						
VIN quiescent current	I_Q	Disable all channels via the I^2C		1	2	mA
V_{IN} under-voltage lockout (UVLO) rising threshold	V_{IN_UVLO}		2.5	2.8	3.1	V
V_{IN} UVLO hysteresis	$V_{IN_UVLO_HYS}$			150		mV
V_{IN} start level (8)	V_{IN_START}	D2h, bits[3:2] = 2'b01	3.7	4	4.3	V
		D2h, bits[3:2] = 2'b10	4.7	5	5.3	
		D2h, bits[3:2] = 2'b11	5.7	6	6.3	
V_{IN} stop level (8)	V_{IN_STOP}	D2h, bits[1:0] = 2'b01	3.2	3.5	3.8	V
		D2h, bits[1:0] = 2'b10	4.2	4.5	4.8	
		D2h, bits[1:0] = 2'b11	5.2	5.5	5.8	
VCC regulation voltage	V_{CC}	C_{VCC} = 4.7µF	4.85	5	5.15	V
V_{CC} UVLO rising threshold	V_{VCC_UVLO}			2.6		V
V_{CC} UVLO hysteresis	V_{VCC_HYS}			200		mV
Oscillator						
Switching frequency (8)	f_{SW}	D1h, bit[1] = 1'b0	1.9	2.2	2.5	MHz
		D1h, bit[1] = 1'b1	2.9	3.3	3.7	
Minimum on time (7)	t_{ON_MIN}			48		ns
Minimum off time (7)	t_{OFF_MIN}			40		ns
Buck Converter 1 (Buck 1)						
Buck 1 output voltage (V_{OUT1}) accuracy	V_{OUT1_ACC}	T_J = 25°C	-1		+1	%
			-1.5		+1.5	%
Buck 1 high-side MOSFET (HS-FET) on resistance	$R_{DS_HS_BUCK1}$			280	500	mΩ
Buck 1 low-side MOSFET (LS-FET) on resistance	$R_{DS_LS_BUCK1}$			150	250	mΩ
SW1 HS-FET leakage current	$I_{ILEAK_HS_BUCK1}$			0.01	1.5	µA
SW1 LS-FET leakage current	$I_{ILEAK_LS_BUCK1}$			12.5	25	µA
SW1 peak current limit (8)	$I_{LIM0_HS_BUCK1}$	D1h, bit[0] = 1'b0	800	1000	1250	mA
	$I_{LIM1_HS_BUCK1}$	D1h, bit[0] = 1'b1	1000	1200	1650	mA
SW1 valley current limit (8)	I_{VALLEY_BUCK1}	D1h, bit[0] = 1'b0	650	850	1100	mA
	I_{VALLEY_BUCK1}	D1h, bit[0] = 1'b1	800	1100	1400	mA
SW1 zero-current detection (ZCD) current	I_{ZCD_BUCK1}		-20	+50	+150	mA
SW1 reverse current limit	I_{REV_BUCK1}		600			mA
V_{OUT1} feedback leakage	I_{FB_BUCK1}	V_{OUT1} = 4V, buck 3 and LDO disabled		35	80	µA
V_{OUT1} output discharge	I_{DIS_BUCK1}	V_{OUT1} = 0.3V	2			mA
Buck 1 soft-start range (7)(8)	t_{SS_BUCK1}		0.5		2.25	ms

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 8V, T_J = -40°C to +150°C, typical values are at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Buck Converter 2 (Buck 2)						
Buck 2 output voltage (V_{OUT2}) accuracy	V_{OUT2_ACC}	$V_{OUT\ 2}$≥ 1.25V, T_J = 25°C	-1		+1	%
		V_{OUT2} ≥ 1.25V	-1.5		+1.5	
	V_{OUT2_ACC}	V_{OUT2} < 1.25V, T_J = 25°C	-1.5		+1.5	%
		V_{OUT2} < 1.25V	-2		+2	
Buck 2 HS-FET on resistance	$R_{DS_HS_BUCK2}$			280	500	mΩ
Buck 2 LS-FET on resistance	$R_{DS_LS_BUCK2}$			150	250	mΩ
SW2 HS-FET leakage current	$I_{ILEAK_HS_BUCK2}$			0.01	1.5	µA
SW2 LS-FET leakage current	$I_{ILEAK_LS_BUCK2}$			10	25	µA
SW2 peak current limit (8)	$I_{LIM0_HS_BUCK2}$	D1h, bit[0] = 1'b0	800	1000	1250	mA
	$I_{LIM1_HS_BUCK2}$	D1h, bit[0] = 1'b1	1000	1250	1650	mA
SW2 valley current limit (8)	I_{VALLEY_BUCK2}	D1h, bit[0] = 1'b0	650	850	1100	mA
	I_{VALLEY_BUCK2}	D1h, bit[0] = 1'b1	800	1100	1400	mA
SW2 ZCD current	I_{ZCD_BUCK2}		-20	+50	+150	mA
SW2 reverse current limit	I_{REV_BUCK2}		600			mA
V_{OUT2} feedback leakage	I_{FB_BUCK2}	V_{OUT2} = 4V		30	45	µA
V_{OUT2} output discharge	I_{DIS_BUCK2}	V_{OUT2} = 0.3V	2			mA
Buck 2 soft-start range (7) (8)	t_{SS_BUCK2}		0.5		2.25	ms
Buck 2 PG over-voltage (OV) rising threshold (8) (9)	$V_{PG_OVR0_BUCK2}$	CCh, bit[0] = 1'b0, V_{OUT2} = 1.8V	102	104	106	%
	$V_{PG_OVR1_BUCK2}$	CCh, bit[0] = 1'b1, V_{OUT2} = 1.8V	104	106	108	%
Buck 2 PG OV falling threshold (8) (9)	$V_{PG_OVF0_BUCK2}$	CCh, bit[0] = 1'b0, V_{OUT2} = 1.8V	101.4	103.4	105.4	%
	$V_{PG_OVF1_BUCK2}$	CCh, bit[0] = 1'b1, V_{OUT2} = 1.8V	103.4	105.4	107.4	%
Buck 2 PG OV threshold hysteresis (9)	$V_{PG_OV_HYS_BUCK2}$			0.6		%
BUCK2 PG under-voltage (UV) rising threshold (8) (9)	$V_{PG_UVR0_BUCK2}$	CCh, bit[0] = 1'b0, V_{OUT2} = 1.8V	95.1	97.1	99.1	%
	$V_{PG_UVR1_BUCK2}$	CCh, bit[0] = 1'b1, V_{OUT2} = 1.8V	92.6	94.6	96.6	%
Buck 2 PG UV falling threshold (8) (9)	$V_{PG_UVF0_BUCK2}$	CCh, bit[0] = 1'b0, V_{OUT2} = 1.8V	94.5	96.5	98.5	%
	$V_{PG_UVF1_BUCK2}$	CCh, bit[0] = 1'b1, V_{OUT2} = 1.8V	92	94	96	%
Buck 2 PG UV threshold hysteresis (9)	$V_{PG_UV_HYS_BUCK2}$			0.6		%

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 8V, T_J = -40°C to +150°C, typical values are at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Buck Converter 3 (Buck 3)						
Buck 3 output voltage (V_{OUT3}) accuracy	V_{OUT3_ACC}	V_{OUT3} ≥ 1.25V, T_J = 25°C	-1		+1	%
		V_{OUT3} ≥ 1.25V	-1.5		+1.5	%
		V_{OUT3} < 1.25V, T_J = 25°C	-1.5		+1.5	%
		V_{OUT3} < 1.25V	-2		+2	%
V_{OUT3} HS-FET on resistance	$R_{DS_HS_BUCK3}$	V_{OUT1} = 4V		115	215	mΩ
V_{OUT3} LS-FET on resistance	$R_{DS_LS_BUCK3}$	V_{OUT1} = 4V		50	110	mΩ
SW3 HS-FET leakage current	$I_{ILEAK_HS_BUCK3}$			0.01	80	µA
SW3 LS-FET leakage current	$I_{ILEAK_LS_BUCK3}$			0.01	10	µA
SW3 peak current limit (8)	$I_{LIM0_HS_BUCK3}$	D1h, bit[0] = 1'b0	1.4	1.65	1.9	A
	$I_{LIM1_HS_BUCK3}$	D1h, bit[0] = 1'b1	1.7	2.1	2.5	A
SW3 valley current limit	I_{VALLEY_BUCK3}		1.2	1.7	2.2	A
SW3 ZCD current	I_{ZCD_BUCK3}		-50	+60	+200	mA
SW3 reverse current limit	I_{REV_BUCK3}		0.6			A
V_{OUT3} feedback leakage	I_{FB_BUCK3}	V_{OUT3} = 2.7V		30	50	µA
V_{OUT3} output discharge	I_{DIS_BUCK3}	V_{OUT3} = 0.3V	2			mA
Buck 3 soft-start range (7)(8)	t_{SS_BUCK3}		0.5		2.25	ms
Buck 3 PG OV rising threshold (8) (9)	$V_{PG_OVR0_BUCK3}$	CCh, bit[0] = 1'b0, V_{OUT3} = 1.2V	102	104	106	%
	$V_{PG_OVR1_BUCK3}$	CCh, bit[0] = 1'b1, V_{OUT3} = 1.2V	104	106	108	%
Buck 3 PG OV falling threshold (8) (9)	$V_{PG_OVF0_BUCK3}$	CCh, bit[0] = 1'b0, V_{OUT3} = 1.2V	101.3	103.3	105.3	%
	$V_{PG_OVF1_BUCK3}$	CCh, bit[0] = 1'b1, V_{OUT3} = 1.2V	103.3	105.3	107.3	%
Buck 3 PG OV threshold hysteresis (9)	$V_{PG_OV_HYS_BUCK3}$			0.7		%
Buck 3 PG under-voltage (UV) rising threshold (8) (9)	$V_{PG_UVR0_BUCK3}$	CCh, bit[0] = 1'b0, V_{OUT3} = 1.2V	95.1	97.1	99.1	%
	$V_{PG_UVR1_BUCK3}$	CCh, bit[0] = 1'b1, V_{OUT3} = 1.2V	92.7	94.7	96.7	%
BUCK3 PG UV falling threshold (8) (9)	$V_{PG_UVF0_BUCK3}$	CCh, bit[0] = 1'b0, V_{OUT3} = 1.2V	94.4	96.4	98.4	%
	$V_{PG_UVF1_BUCK3}$	CCh, bit[0] = 1'b1, V_{OUT3} = 1.2V	92	94	96	%
BUCK3 PG UV threshold hysteresis (9)	$V_{PG_UV_HYS_BUCK3}$			0.7		%

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 8V, T_J = -40°C to +150°C, typical values are at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Low-Dropout (LDO) Regulator						
LDO accuracy	V_{LDO_ACC}	V_{LDO} ≥ 1.25V, T_J = 25°C	-1		+1	%
		V_{LDO} ≥ 1.25V	-1.5		+1.5	%
		V_{LDO} < 1.25V, T_J = 25°C	-1.5		+1.5	%
		V_{LDO} < 1.25V	-2		+2	%
LDO PSRR (7)	L_{DO_PSRR}	No input capacitor, C_{OUT} = 22µF, f = 2MHz, I_{LDO} = 100mA		50		dB
LDO dropout voltage	V_{DROP_LDO}	V_{IN3} = 3.2V, I_{LDO} = 200mA, setting LDO output = 3.3V		100	220	mV
LDO current limit	I_{LIM_LDO}	V_{IN3} = 3V, setting LDO output = 2.5V	280			mA
LDO output discharge	I_{DIS_LDO}	V_{LDO} = 0.3V	2			mA
LDO soft-start time	t_{SS_B2}	V_{OUT} = 10% to 90%, C_{OUT} = 2.2µF, setting LDO output = 2.5V	50	130	200	µs
LDO line regulation	$L_{DO_LINE_REG}$	V_{IN3} = 2.5V to 4V, V_{LDO} = 2V, I_{LDO} = 10mA		0.02	0.1	%/V
LDO load regulation	$L_{DO_LOAD_REG}$	V_{IN3} = 3.8V, V_{LDO} = 3.3V, I_{OUT} from 10mA to 200mA		0.03	0.15	%
LDO noise (7)	V_{LDO_NOISE}	V_{IN3} = 3.7V, V_{LDO} = 3.3V, I_{LDO} = 200mA, buck 1 not switching, buck 2 and buck 3 disabled		105		μV_{RMS}
LDO PG OV rising threshold (8) (9)	$V_{PG_OVR0_LDO}$	CCh, bit[0] = 1'b0, V_{LDO} = 2.5V	102	104	106	%
	$V_{PG_OVR1_LDO}$	CCh, bit[0] = 1'b1, V_{LDO} = 2.5V	104	106	108	%
LDO PG OV falling threshold (8) (9)	$V_{PG_OVF0_LDO}$	CCh, bit[0] = 1'b0, V_{LDO} = 2.5V	101.4	103.4	105.4	%
	$V_{PG_OVF1_LDO}$	CCh, bit[0] = 1'b1, V_{LDO} = 2.5V	103.4	105.4	107.4	%
LDO PG OV threshold hysteresis (9)	$V_{PG_OV_HYS_LDO}$			0.6		%
LDO PG UV rising threshold (8) (9)	$V_{PG_UVR0_LDO}$	CCh, bit[0] = 1'b0, V_{LDO} = 2.5V	94.6	96.6	98.6	%
	$V_{PG_UVR1_LDO}$	CCh, bit[0] = 1'b1, V_{LDO} = 2.5V	92.6	94.6	96.6	%
LDO PG UV falling threshold (8) (9)	$V_{PG_UVF0_LDO}$	CCh, bit[0] = 1'b0, V_{LDO} = 2.5V	94	96	98	%
	$V_{PG_UVF1_LDO}$	CCh, bit[0] = 1'b1, V_{LDO} = 2.5V	92	94	96	%
LDO PG UV threshold hysteresis (9)	$V_{PG_UV_HYS_LDO}$			0.6		%
Thermal Protection						
Thermal warning (7)	T_{TW}		110	125	140	°C
Thermal warning hysteresis (7)	T_{TW_HYS}			20		°C
Thermal shutdown (7)	T_{SD}		155	170	185	°C
Thermal shutdown hysteresis (7)	T_{SD_HYS}			20		°C

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 8V, T_J = -40°C to +150°C, typical values are at T_J = 25°C, unless otherwise noted

Parameter	Symbol	Condition	Min	Typ	Max	Units
Output Voltage (V_{OUT}) Protection						
V_{OUT} OV threshold (9)	V_{OUT_OV}	V_{OUT} ≥ 1.25V	112	115	118	%
		V_{OUT} < 1.25V	110	115	120	%
V_{OUT} OV hysteresis (9)	$V_{OUT_OV_HYS}$	V_{OUT} ≥ 1.25V	3.5	6	8.5	%
		V_{OUT} < 1.25V	2.5	6	10	%
V_{OUT} UV threshold (9)	V_{OUT_UV}	V_{OUT} ≥ 1.25V	72	75	78	%
		V_{OUT} < 1.25V	70	75	80	%
Hiccup time	t_{HIC}			1		ms
Configuring Options						
V_{OUT} range (7) (8)	V_{OUT1}		2.5		4	V
	V_{OUT2}		0.6		3.75	
	V_{OUT3}		0.6		2.55	
	V_{LDO}		0.6		3.75	
Start delay range (7) (8)	t_{START_DELAY}	Start counting from V_{IN} > V_{IN_START}	0		37.5	ms
Stop delay range (7) (8)	t_{STOP_DELAY}	Start counting from V_{IN} < V_{IN_STOP} or I^2C off command	0		37.5	ms
I^2C Interface (7)						
I^2C ready time	t_{PMB_R}	From V_{IN} > UVLO to I^2C ready			12	ms
Input logic high	V_{IH}		1.7			V
Input logic low	V_{IL}				0.4	V
Output voltage logic low	V_{OUT_L}	SDA pin sink 4mA			0.4	V
SCL clock frequency	f_{SCL}				1000	kHz
SCL high time	t_{HIGH}		260			ns
SCL low time	t_{LOW}		500			ns
Data set-up time	t_{SU_DAT}		50			ns
Data hold time	t_{HD_DAT}		0			ns
Set-up time for repeated start	t_{SU_STA}		260			ns
Hold time for (repeated) start	t_{HD_STA}		260			ns
Bus free time between a start and a stop command	t_{BUF}		500			ns
Set-up time for stop command	t_{SU_STO}		260			ns
Rising time of SCL and SDA	t_R				120	ns
Falling time of SCL and SDA	t_F	V_{DD} supplies the digital interface		20 x (V_{DD} / 5.5V)	120	ns
Pulse width of suppressed spike	t_{SP}				50	ns
Capacitance bus for each bus line	C_B				550	pF

Notes:

9) Guaranteed by design and bench characterization. Not tested in production.

8) Update these EC parameters by writing to the register map. See the Register Map section starting on page 40 for detailed descriptions.

9) The threshold is based on the nominal output voltage of each output.

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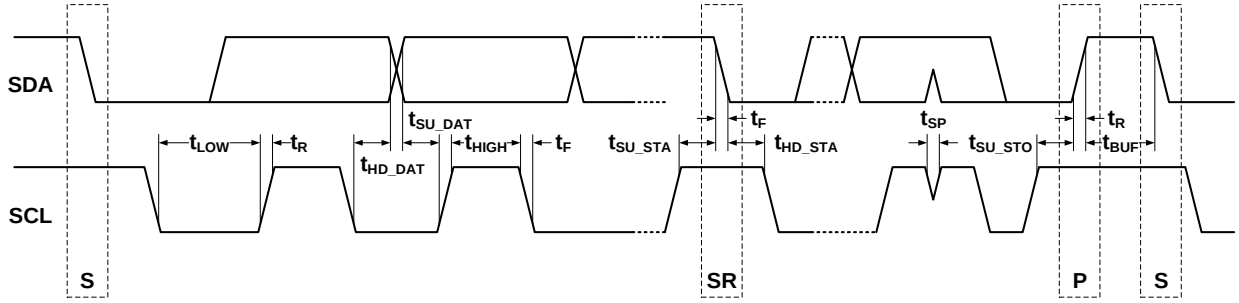
I²C-COMPATIBLE INTERFACE TIMING DIAGRAM



S: Start Command

SR: Repeated Start Command

P: Stop Command

Figure 1: I²C-Compatible Interface Timing Diagram

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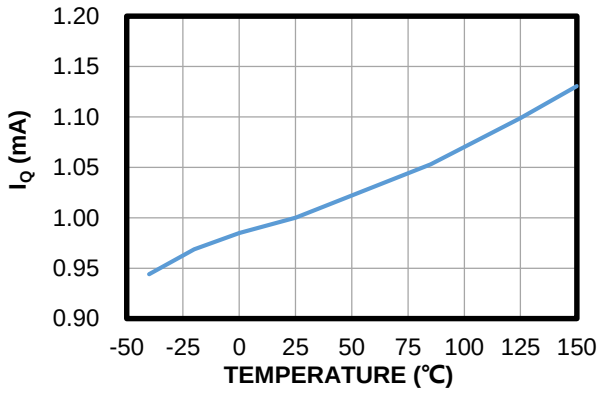
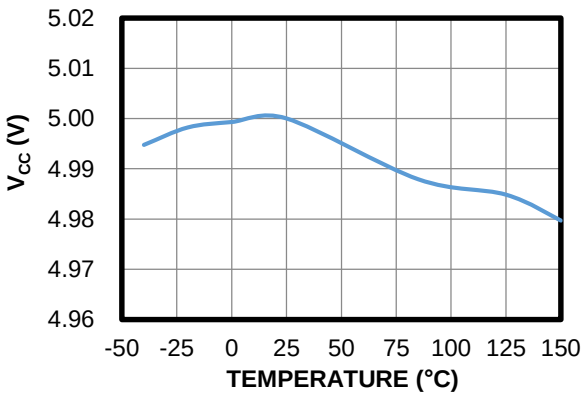
TYPICAL CHARACTERISTICS

V_{IN} = 8V, T_A = -40°C to +150°C, unless otherwise noted.

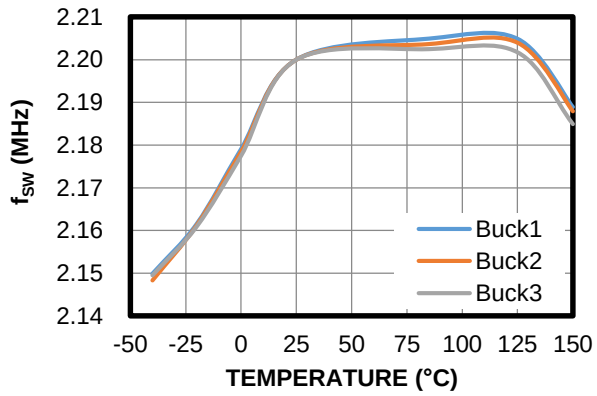
I_Q vs. Temperature



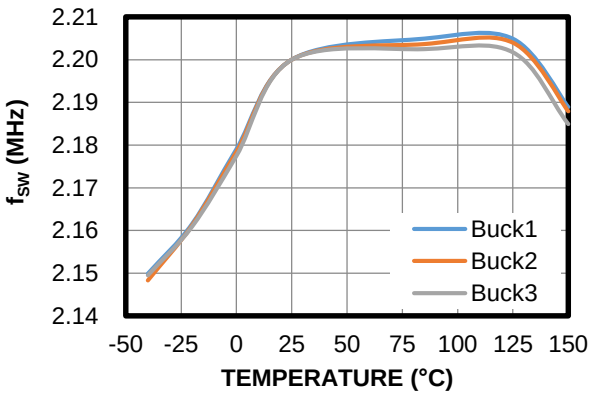
V_{CC} vs. Temperature



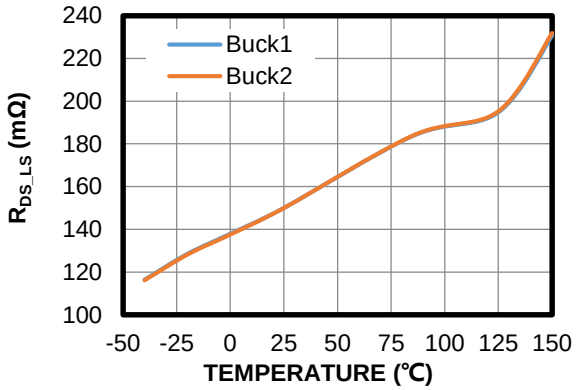
f_{SW} vs. Temperature



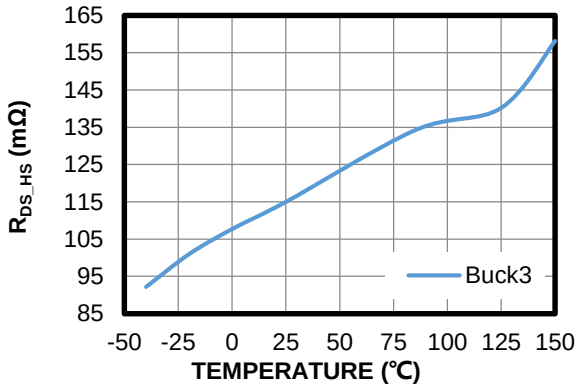
f_{SW} vs. Temperature



R_{DS_LS} vs. Temperature



R_{DS_HS} vs. Temperature



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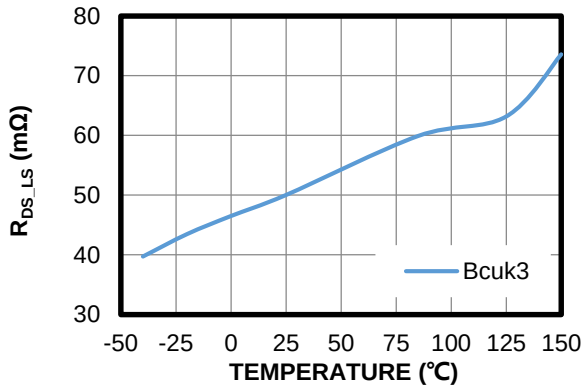
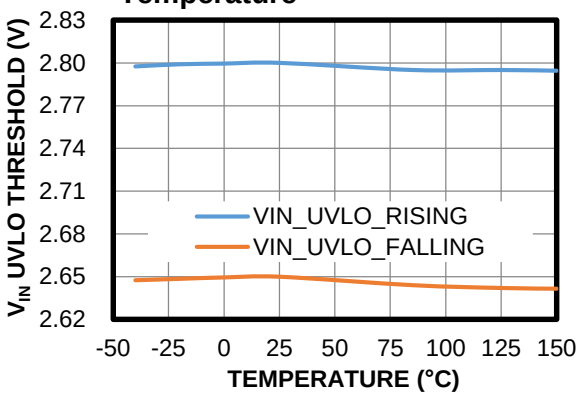
TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 8V, T_A = -40°C to +150°C, unless otherwise noted.

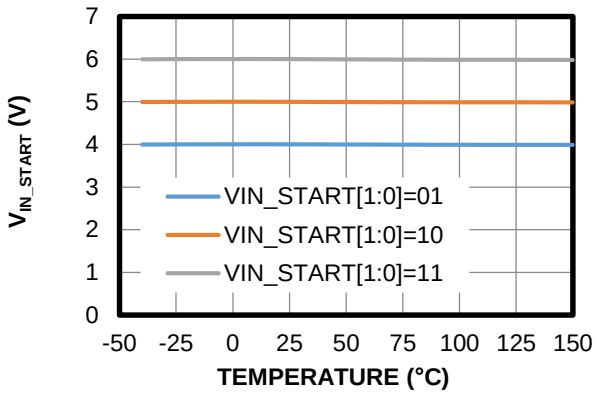
R_{DS_LS} vs. Temperature



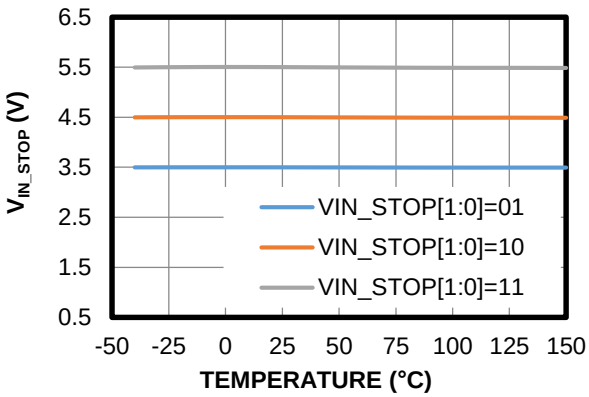
V_{IN} UVLO Threshold vs. Temperature



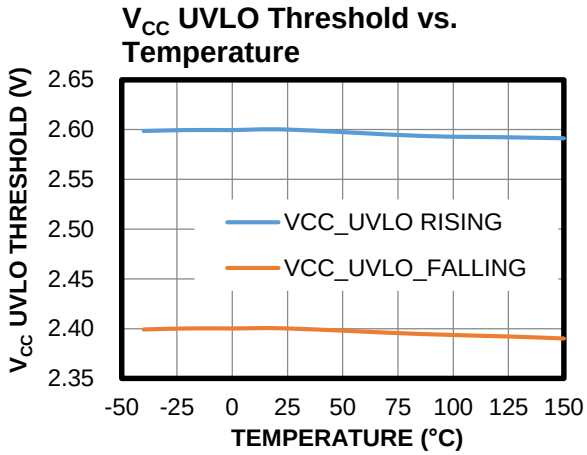
V_{IN_START} vs.Temperature



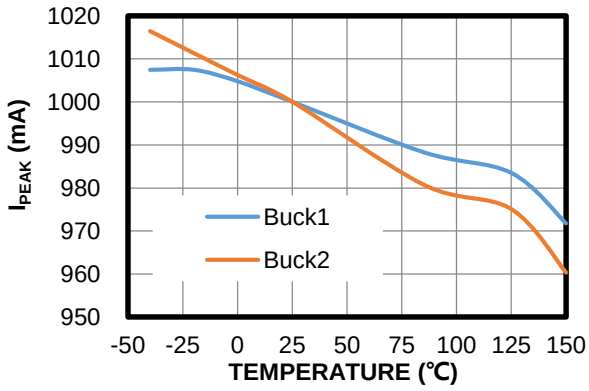
V_{IN_STOP} vs. Temperature



V_{CC} UVLO Threshold vs. Temperature



I_{PEAK} vs. Temperature



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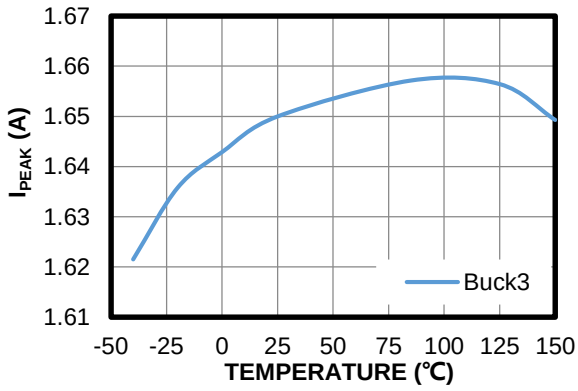
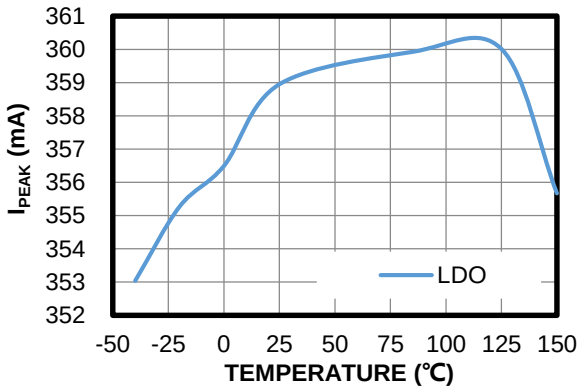
TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 8V, T_A = -40°C to +150°C, unless otherwise noted.

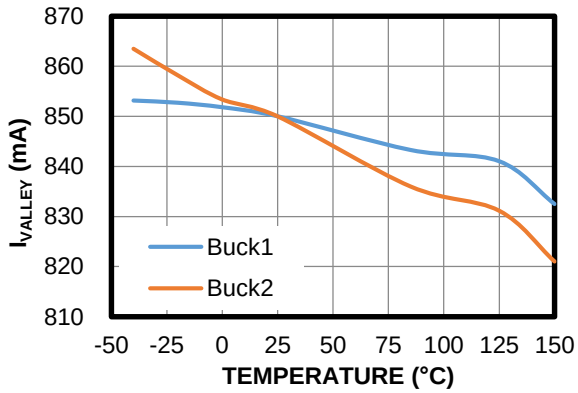
I_{PEAK} vs. Temperature



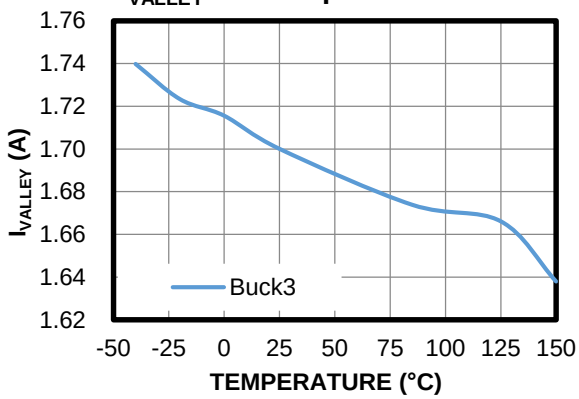
I_{PEAK} vs. Temperature



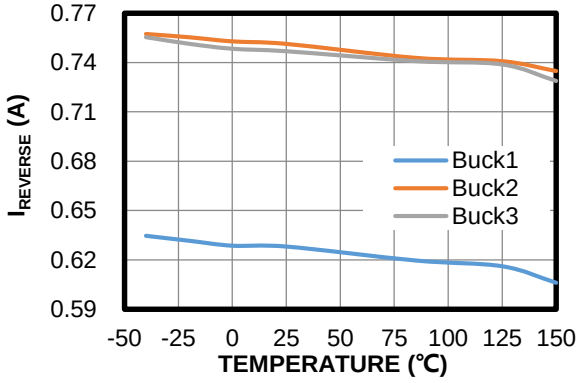
I_{VALLEY} vs. Temperature



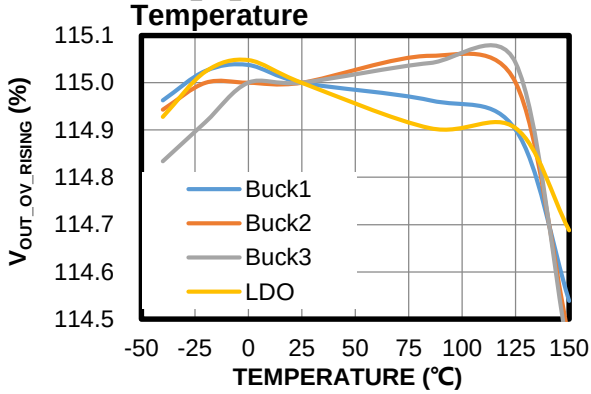
I_{VALLEY} vs. Temperature



$I_{REVERSE}$ vs. Temperature



$V_{OUT_OV_RISING}$ vs. Temperature



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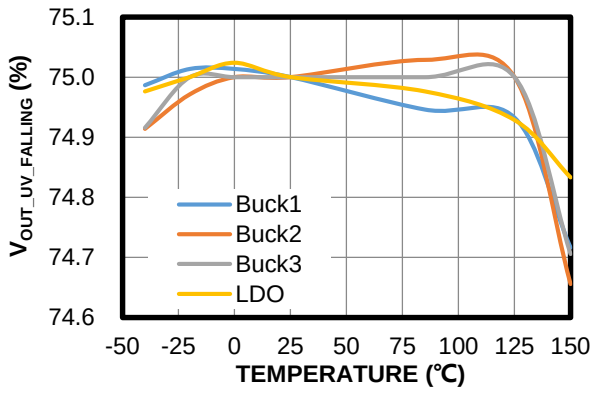
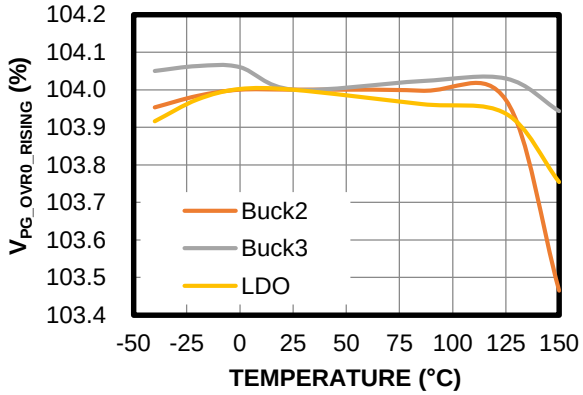
TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 8V, T_A = -40°C to +150°C, unless otherwise noted.

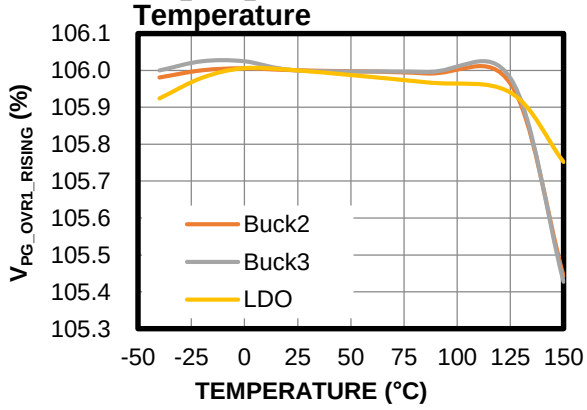
$V_{OUT_UV_FALLING}$ vs. Temperature



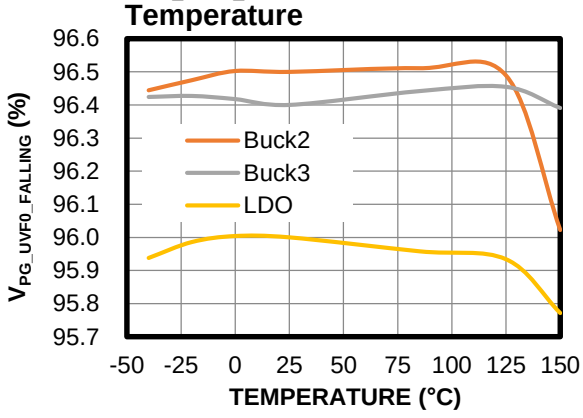
$V_{PG_OVR0_RISING}$ vs. Temperature



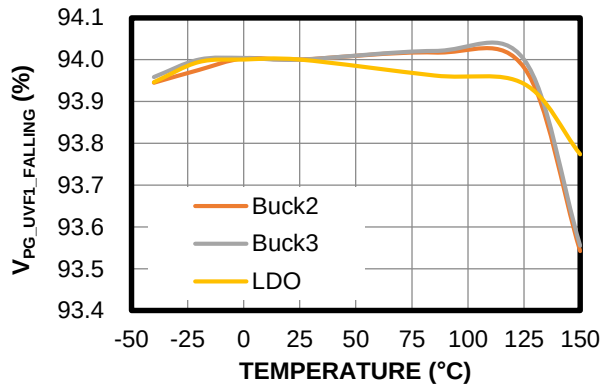
$V_{PG_OVR1_RISING}$ vs. Temperature



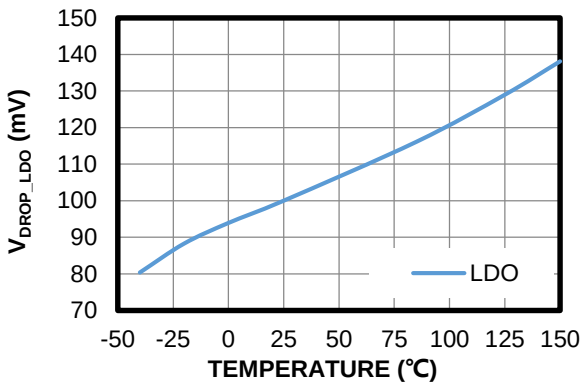
$V_{PG_UVF0_FALLING}$ vs. Temperature



$V_{PG_UVF1_FALLING}$ vs. Temperature



V_{DROP_LDO} vs. Temperature



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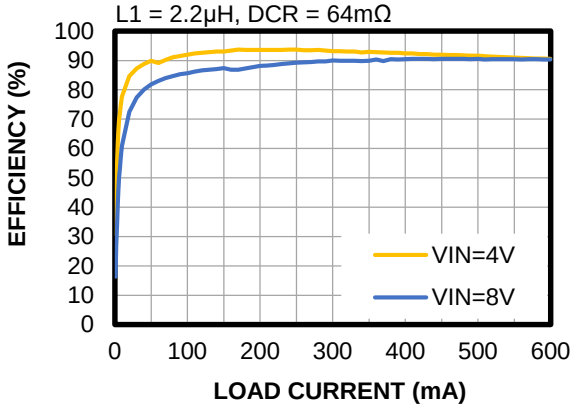
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 8V, V_{OUT1} = 3V, V_{OUT2} = 1.8V, V_{OUT3} = 1.2V, V_{LDO} = 2.5V, L1 = L2 = 2.2µH, L3 = 1µH, f_{SW1} = f_{SW2} = f_{SW3} = 2.2MHz, FCCM, T_A = 25°C, unless otherwise noted.

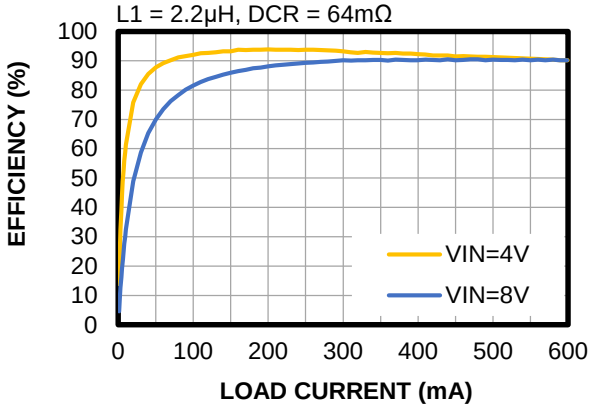
Efficiency vs. Load Current (Buck 1)

V_{OUT1} = 3V, f_{SW1} = 2.2MHz, DCM, other channels are disabled, L1 = 2.2µH, DCR = 64mΩ



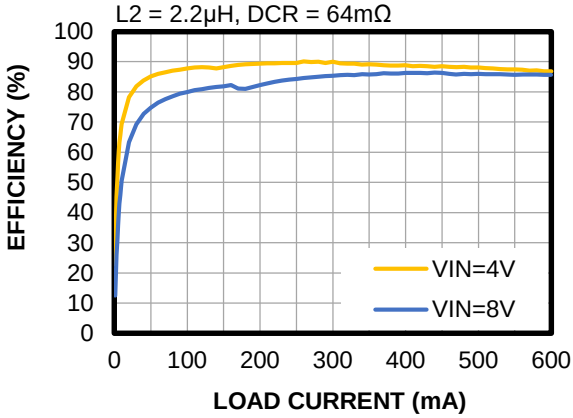
Efficiency vs. Load Current (Buck 1)

V_{OUT1} = 3V, f_{SW1} = 2.2MHz, FCCM, other channels are disabled, L1 = 2.2µH, DCR = 64mΩ



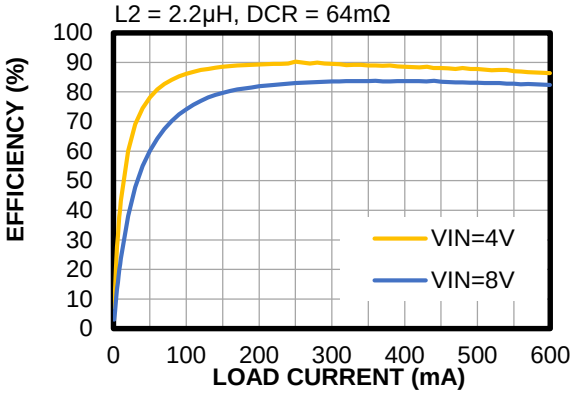
Efficiency vs. Load Current (Buck 2)

V_{OUT2} = 1.8V, f_{SW2} = 2.2MHz, DCM, other channels are disabled, L2 = 2.2µH, DCR = 64mΩ



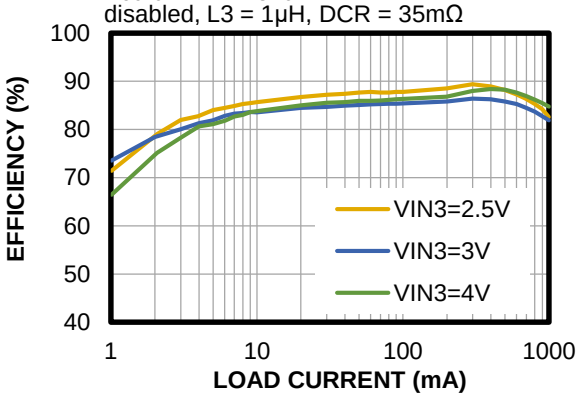
Efficiency vs. Load Current (Buck 2)

V_{OUT2} = 1.8V, f_{SW2} = 2.2MHz, FCCM, other channels are disabled, L2 = 2.2µH, DCR = 64mΩ



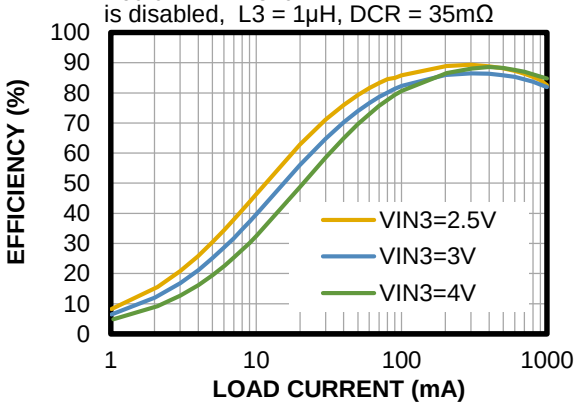
Efficiency vs. Load Current (Buck 3)

V_{OUT3} = 1.2V, f_{SW3} = 2.2MHz, DCM, LDO is disabled, L3 = 1µH, DCR = 35mΩ



Efficiency vs. Load Current (Buck 3)

V_{OUT3} = 1.2V, f_{SW3} = 2.2MHz, FCCM, LDO is disabled, L3 = 1µH, DCR = 35mΩ



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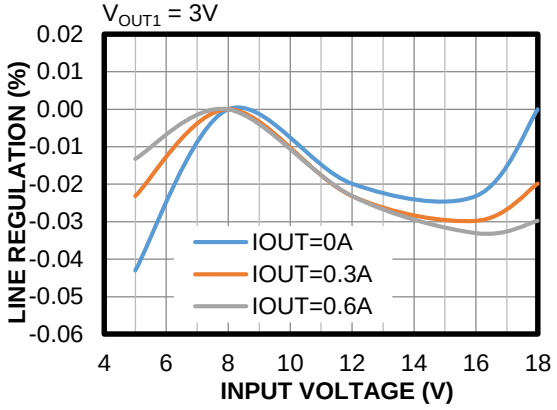
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 8V, V_{OUT1} = 3V, V_{OUT2} = 1.8V, V_{OUT3} = 1.2V, V_{LDO} = 2.5V, L1 = L2 = 2.2µH, L3 = 1µH, f_{SW1} = f_{SW2} = f_{SW3} = 2.2MHz, FCCM, T_A = 25°C, unless otherwise noted.

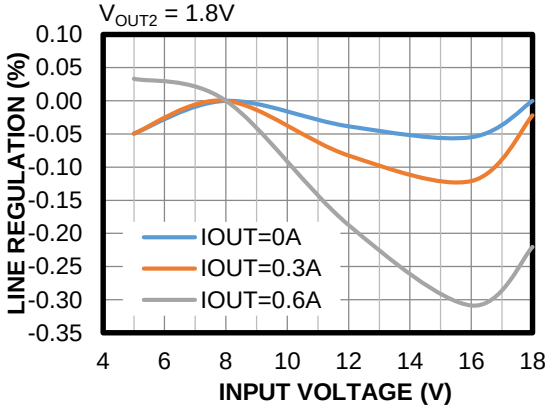
Line Regulation (Buck 1)

V_{OUT1} = 3V



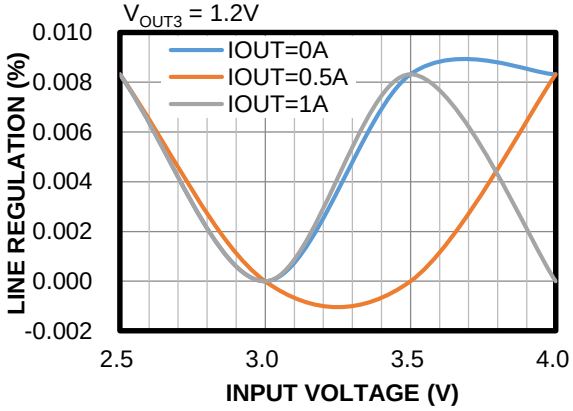
Line Regulation (Buck 2)

V_{OUT2} = 1.8V



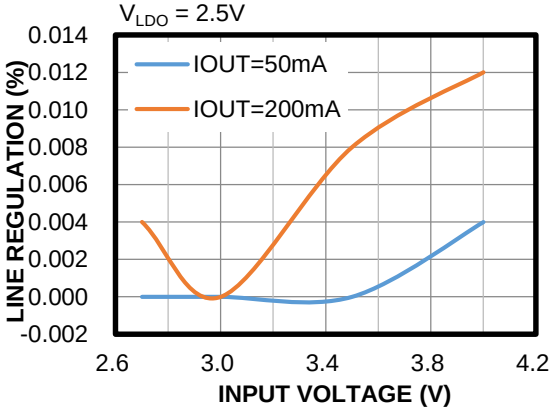
Line Regulation (Buck 3)

V_{OUT3} = 1.2V



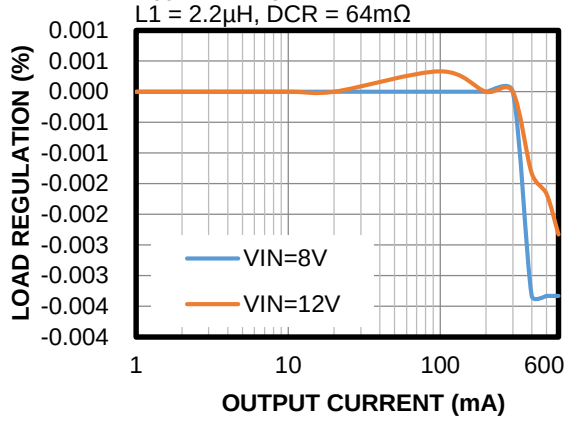
Line Regulation (LDO)

V_{LDO} = 2.5V



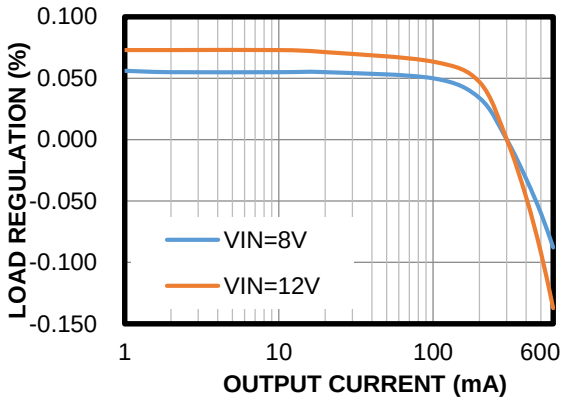
Load Regulation (Buck 1)

V_{OUT1} = 3V, f_{SW1} = 2.2MHz, FCCM,
L1 = 2.2µH, DCR = 64mΩ



Load Regulation (Buck 2)

V_{OUT2} = 1.8V, f_{SW2} = 2.2MHz, FCCM,
L2 = 2.2µH, DCR = 64mΩ



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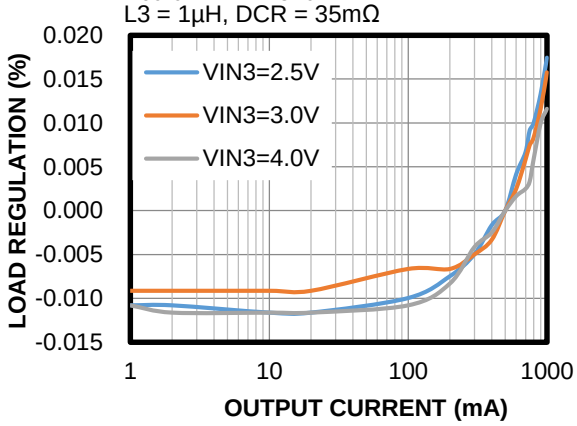
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 8V, V_{OUT1} = 3V, V_{OUT2} = 1.8V, V_{OUT3} = 1.2V, V_{LDO} = 2.5V, L1 = L2 = 2.2µH, L3 = 1µH, f_{SW1} = f_{SW2} = f_{SW3} = 2.2MHz, FCCM, T_A = 25°C, unless otherwise noted.

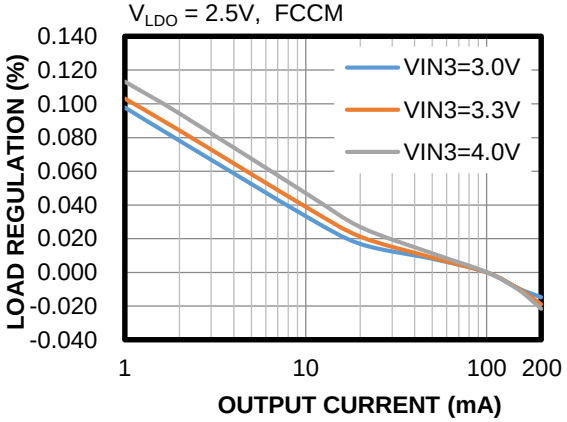
Load Regulation (Buck 3)

V_{OUT3} = 1.2V, f_{SW3} = 2.2MHz, FCCM, L3 = 1µH, DCR = 35mΩ



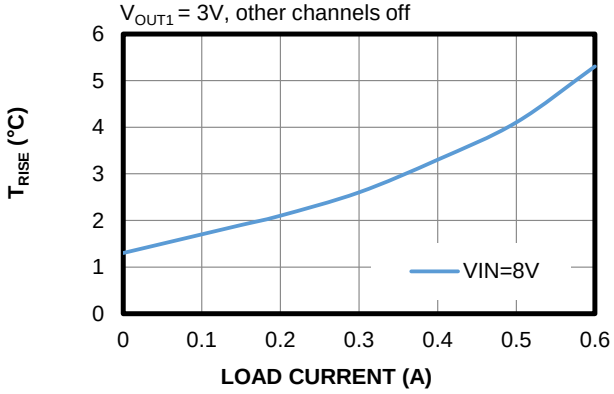
Load Regulation (LDO)

V_{LDO} = 2.5V, FCCM



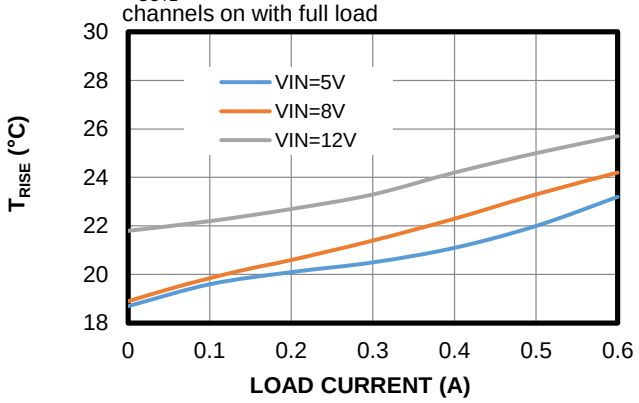
Case Thermal Rise (Buck 1)

V_{OUT1} = 3V, other channels off



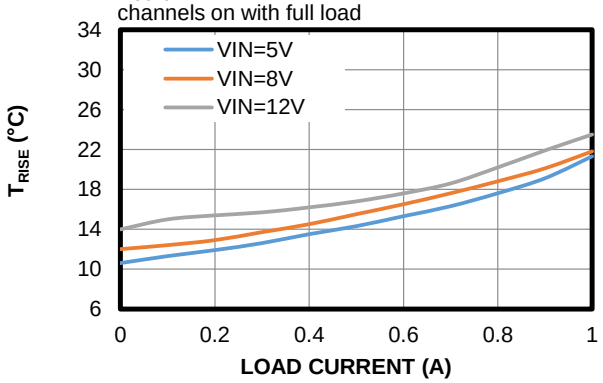
Case Thermal Rise (Buck 2)

V_{OUT2} = 1.8V, channel 1 on with no load, other channels on with full load



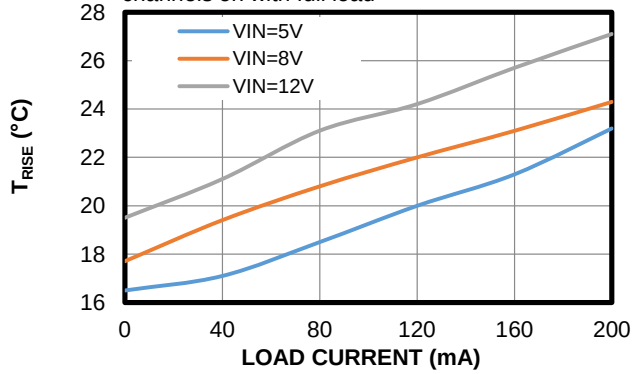
Case Thermal Rise (Buck 3)

V_{OUT3} = 1.2V, channel 1 on with no load, other channels on with full load



Case Thermal Rise (LDO)

V_{LDO} = 2.5V, channel 1 on with no load, other channels on with full load



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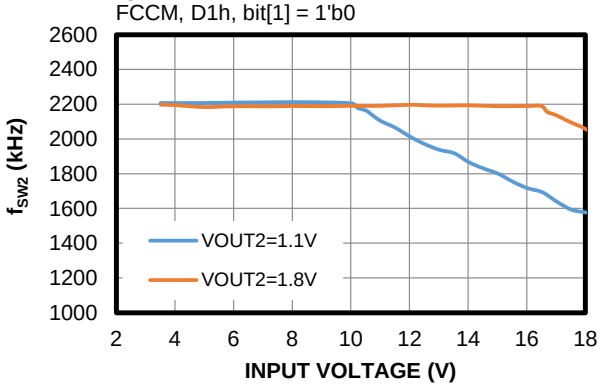
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 8V, V_{OUT1} = 3V, V_{OUT2} = 1.8V, V_{OUT3} = 1.2V, V_{LDO} = 2.5V, L1 = L2 = 2.2µH, L3 = 1µH, f_{SW1} = f_{SW2} = f_{SW3} = 2.2MHz, FCCM, T_A = 25°C, unless otherwise noted.

f_{SW2} vs. V_{IN}
FCCM, D1h, bit[1] = 1'b0



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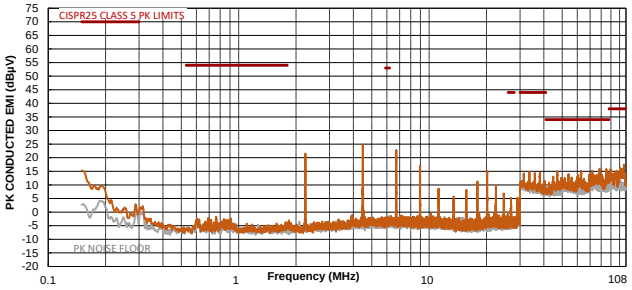
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 8V, V_{OUT1} = 3V, V_{OUT2} = 1.8V, V_{OUT3} = 1.2V, V_{LDO} = 2.5V, L1 = L2 = 2.2µH, L3 = 1µH, f_{SW1} = f_{SW2} = f_{SW3} = 2.2MHz, FCCM, T_A = 25°C, unless otherwise noted. (10)

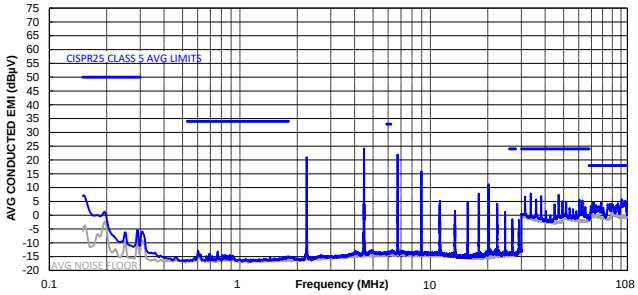
CISPR25 Class 5 Peak Conducted Emissions

150kHz to 108MHz



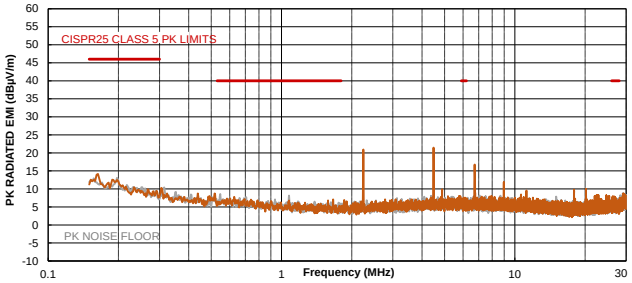
CISPR25 Class 5 Average Conducted Emissions

150kHz to 108MHz



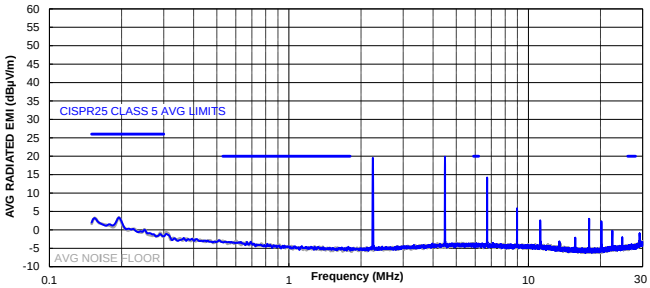
CISPR25 Class 5 Peak Radiated Emissions

150kHz to 30MHz



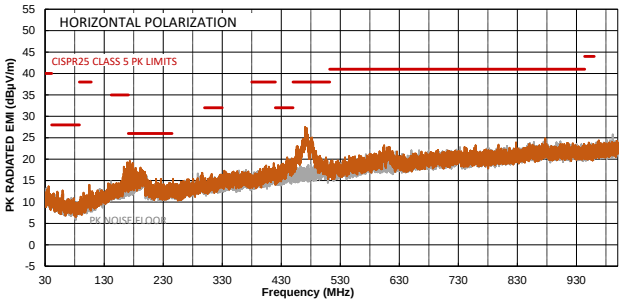
CISPR25 Class 5 Average Radiated Emissions

150kHz to 30MHz



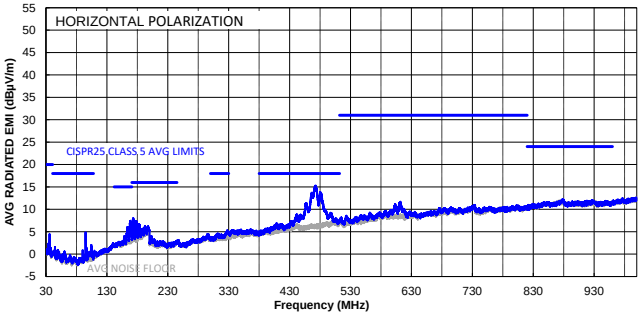
CISPR25 Class 5 Peak Radiated Emissions

Horizontal, 30MHz to 1GHz



CISPR25 Class 5 Average Radiated Emissions

Horizontal, 30MHz to 1GHz



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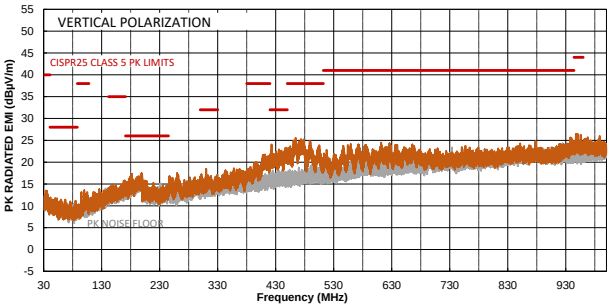
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 8V, V_{OUT1} = 3V, V_{OUT2} = 1.8V, V_{OUT3} = 1.2V, V_{LDO} = 2.5V, L1 = L2 = 2.2µH, L3 = 1µH, f_{SW1} = f_{SW2} = f_{SW3} = 2.2MHz, FCCM, T_A = 25°C, unless otherwise noted. (10)

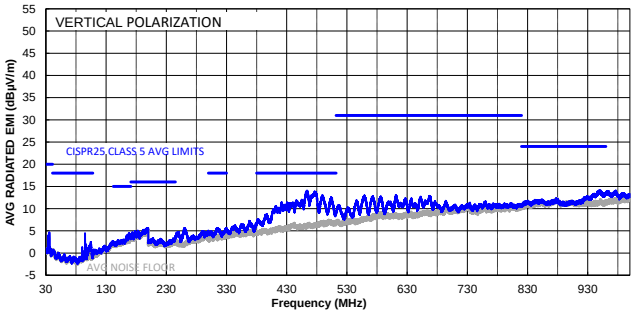
CISPR25 Class 5 Peak Radiated Emissions

Vertical, 30MHz to 1GHz



CISPR25 Class 5 Average Radiated Emissions

Vertical, 30MHz to 1GHz



Note:

10) The EMC test results are based on the application circuit with EMI filters and no FSS function (see Figure 15 on page 66).

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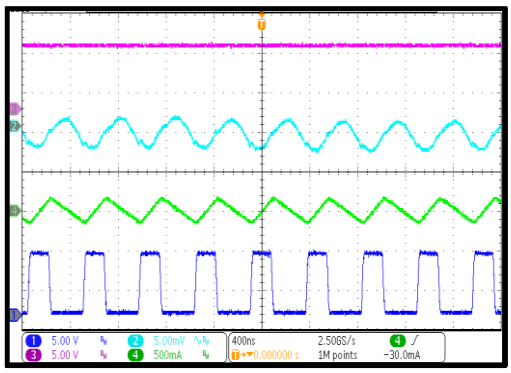
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 8V, V_{OUT1} = 3V, V_{OUT2} = 1.8V, V_{OUT3} = 1.2V, V_{LDO} = 2.5V, L1 = L2 = 2.2µH, L3 = 1µH, f_{SW1} = f_{SW2} = f_{SW3} = 2.2MHz, FCCM, T_A = 25°C, unless otherwise noted.

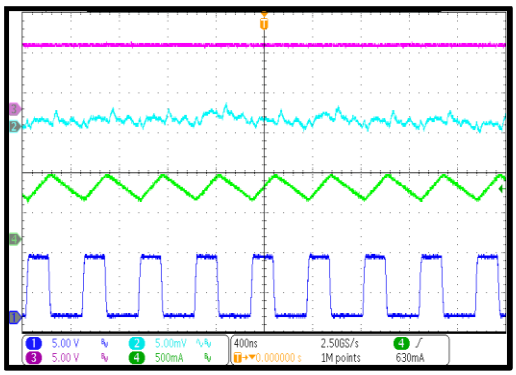
Steady State (Buck 1)

I_{OUT1} = I_{OUT2} = I_{OUT3} = I_{LDO} = 0A



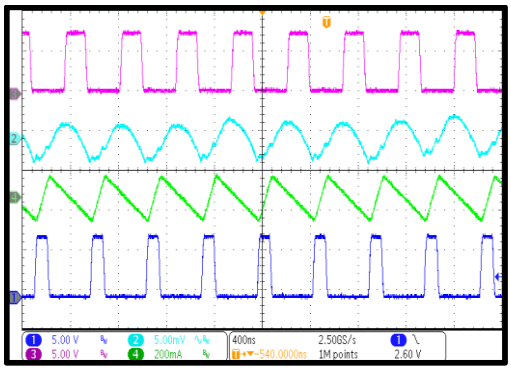
Steady State (Buck 1)

I_{OUT1} = 0A, I_{OUT2} = 600mA, I_{OUT3} = 1A, I_{LDO} = 200mA



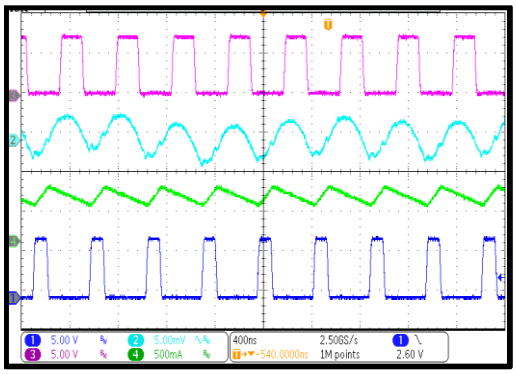
Steady State (Buck 2)

I_{OUT1} = I_{OUT2} = I_{OUT3} = I_{LDO} = 0A



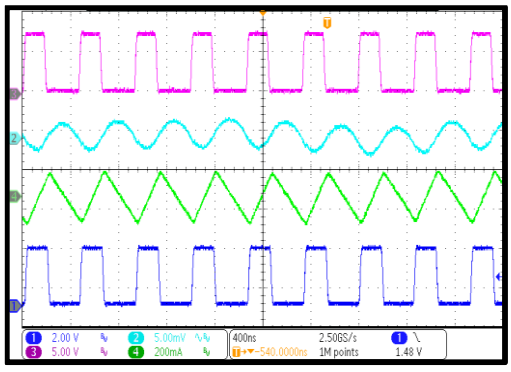
Steady State (Buck 2)

I_{OUT1} = 0A, I_{OUT2} = 600mA, I_{OUT3} = 1A, I_{LDO} = 200mA



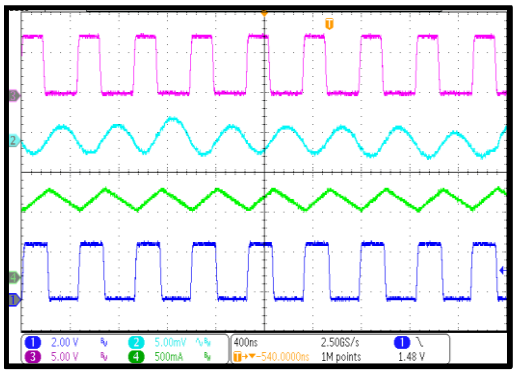
Steady State (Buck 3)

I_{OUT1} = I_{OUT2} = I_{OUT3} = I_{LDO} = 0A



Steady State (Buck 3)

I_{OUT1} = 0A, I_{OUT2} = 600mA, I_{OUT3} = 1A, I_{LDO} = 200mA



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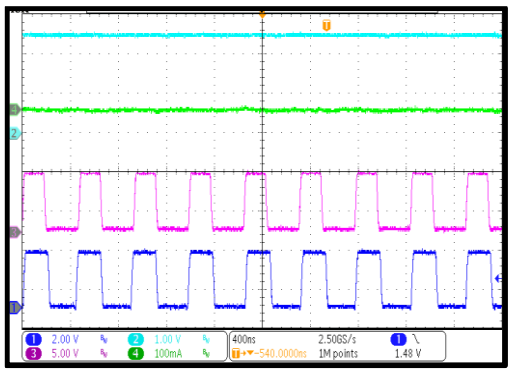
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 8V, V_{OUT1} = 3V, V_{OUT2} = 1.8V, V_{OUT3} = 1.2V, V_{LDO} = 2.5V, L1 = L2 = 2.2µH, L3 = 1µH, f_{SW1} = f_{SW2} = f_{SW3} = 2.2MHz, FCCM, T_A = 25°C, unless otherwise noted.

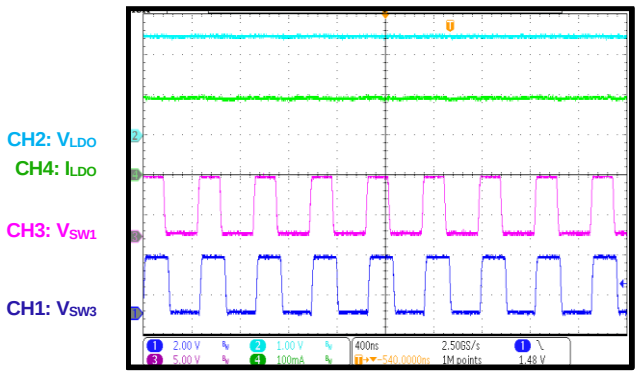
Steady State (LDO)

I_{OUT1} = I_{OUT2} = I_{OUT3} = I_{LDO} = 0A



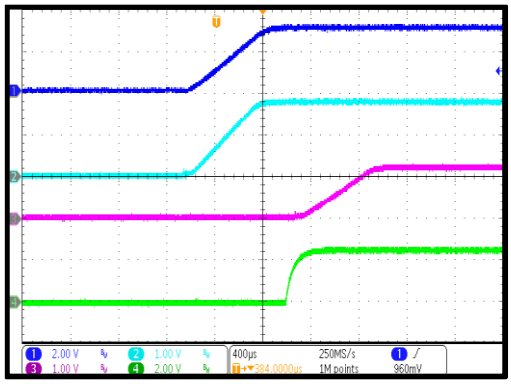
Steady State (LDO)

I_{OUT1} = 0A, I_{OUT2} = 600mA, I_{OUT3} = 1A, I_{LDO} = 200mA



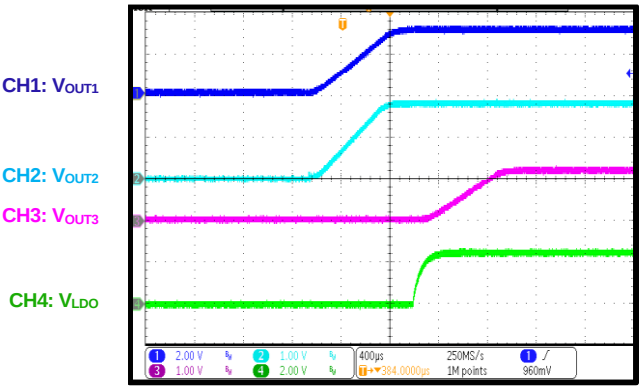
Start-Up through VIN (Start-Up Sequence)

I_{OUT1} = I_{OUT2} = I_{OUT3} = I_{LDO} = 0A



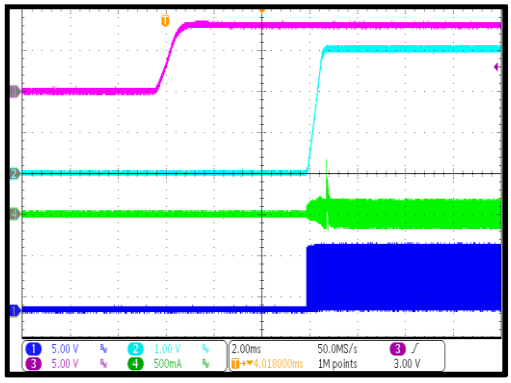
Start-Up through VIN (Start-Up Sequence)

I_{OUT1} = 0A, I_{OUT2} = 600mA, I_{OUT3} = 1A, I_{LDO} = 200mA



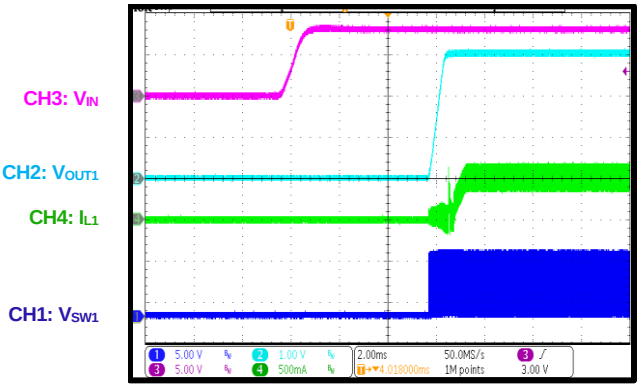
Start-Up through VIN (Buck 1)

I_{OUT1} = I_{OUT2} = I_{OUT3} = I_{LDO} = 0A



Start-Up through VIN (Buck 1)

I_{OUT1} = 0A, I_{OUT2} = 600mA, I_{OUT3} = 1A, I_{LDO} = 200mA



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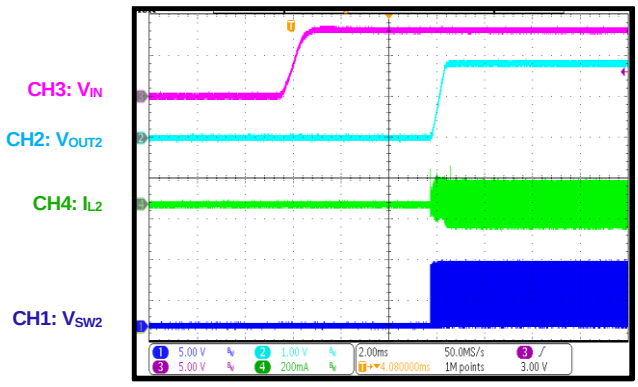
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 8V, V_{OUT1} = 3V, V_{OUT2} = 1.8V, V_{OUT3} = 1.2V, V_{LDO} = 2.5V, L1 = L2 = 2.2µH, L3 = 1µH, f_{SW1} = f_{SW2} = f_{SW3} = 2.2MHz, FCCM, T_A = 25°C, unless otherwise noted.

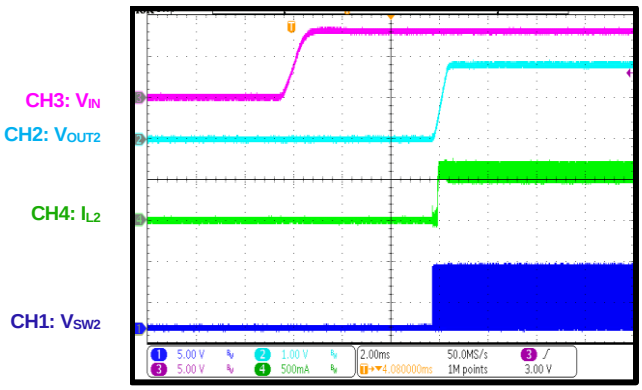
Start-Up through VIN (Buck 2)

I_{OUT1} = I_{OUT2} = I_{OUT3} = I_{LDO} = 0A



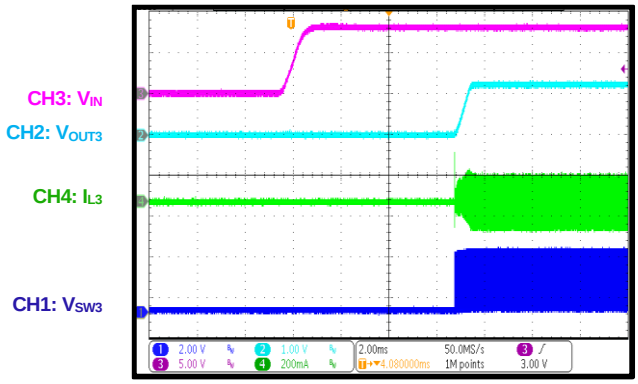
Start-Up through VIN (Buck 2)

I_{OUT1} = 0A, I_{OUT2} = 600mA, I_{OUT3} = 1A, I_{LDO} = 200mA



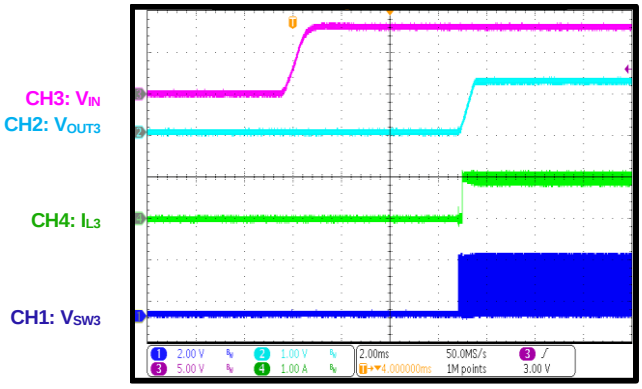
Start-Up through VIN (Buck 3)

I_{OUT1} = I_{OUT2} = I_{OUT3} = I_{LDO} = 0A



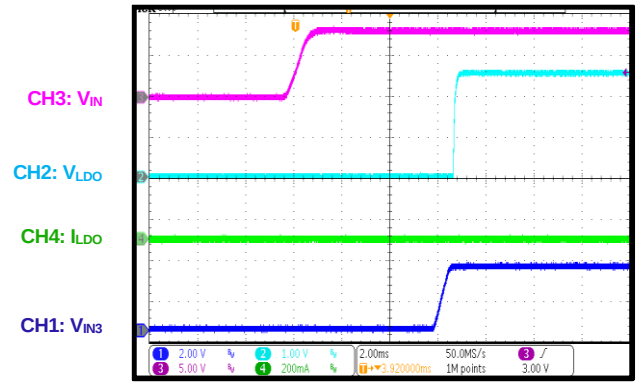
Start-Up through VIN (Buck 3)

I_{OUT1} = 0A, I_{OUT2} = 600mA, I_{OUT3} = 1A, I_{LDO} = 200mA



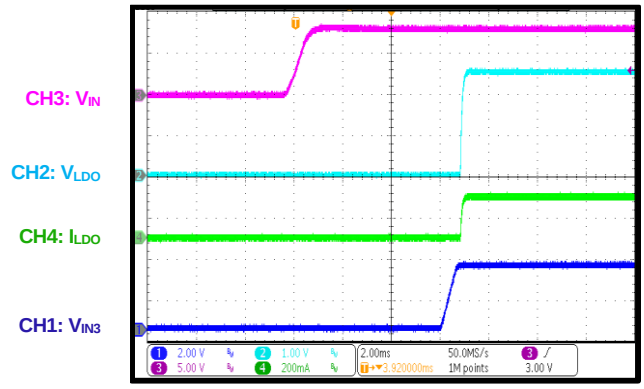
Start-Up through VIN (LDO)

I_{OUT1} = I_{OUT2} = I_{OUT3} = I_{LDO} = 0A



Start-Up through VIN (LDO)

I_{OUT1} = 0A, I_{OUT2} = 600mA, I_{OUT3} = 1A, I_{LDO} = 200mA



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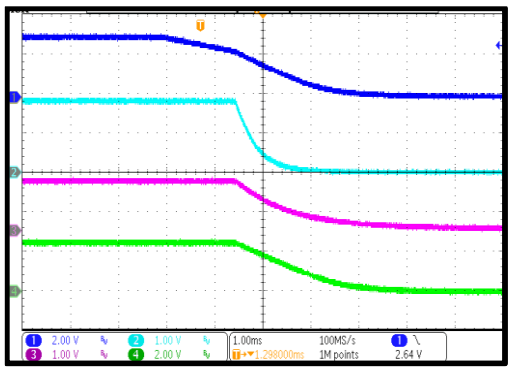
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 8V, V_{OUT1} = 3V, V_{OUT2} = 1.8V, V_{OUT3} = 1.2V, V_{LDO} = 2.5V, L1 = L2 = 2.2µH, L3 = 1µH, f_{SW1} = f_{SW2} = f_{SW3} = 2.2MHz, FCCM, T_A = 25°C, unless otherwise noted.

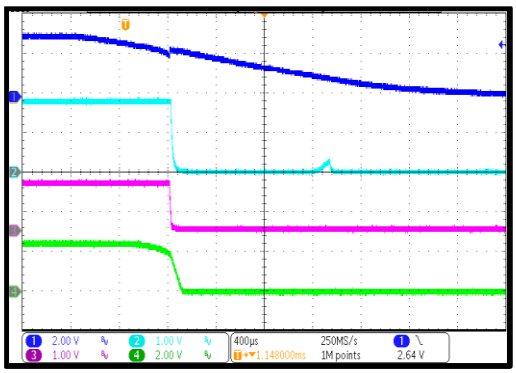
Shutdown through VIN

I_{OUT1} = I_{OUT2} = I_{OUT3} = I_{LDO} = 0A



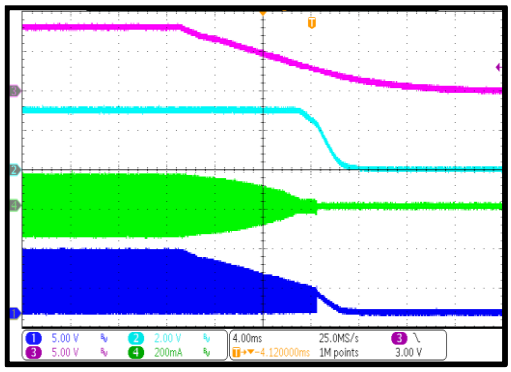
Shutdown through VIN

I_{OUT1} = 0A, I_{OUT2} = 600mA, I_{OUT3} = 1A, I_{LDO} = 200mA



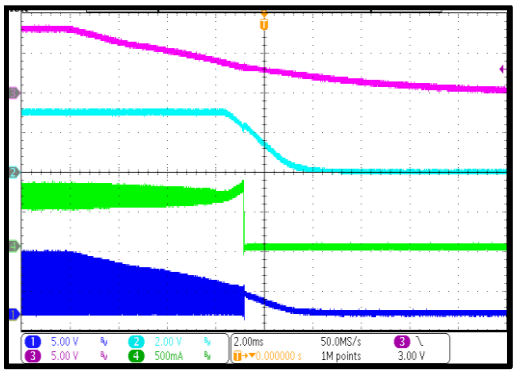
Shutdown through VIN (Buck1)

I_{OUT1} = I_{OUT2} = I_{OUT3} = I_{LDO} = 0A



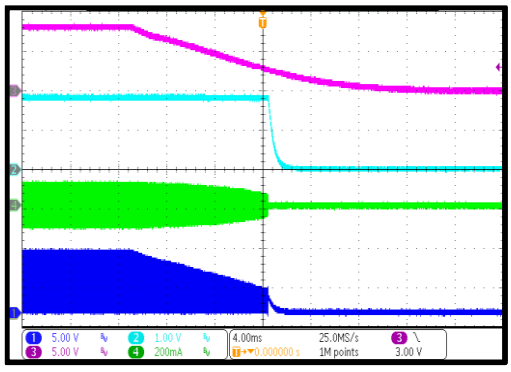
Shutdown through VIN (Buck1)

I_{OUT1} = 0A, I_{OUT2} = 600mA, I_{OUT3} = 1A, I_{LDO} = 200mA



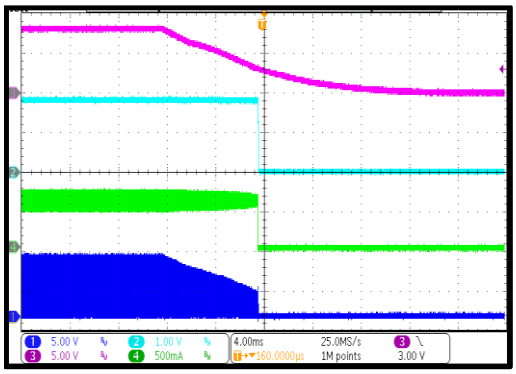
Shutdown through VIN (Buck 2)

I_{OUT1} = I_{OUT2} = I_{OUT3} = I_{LDO} = 0A



Shutdown through VIN (Buck 2)

I_{OUT1} = 0A, I_{OUT2} = 600mA, I_{OUT3} = 1A, I_{LDO} = 200mA



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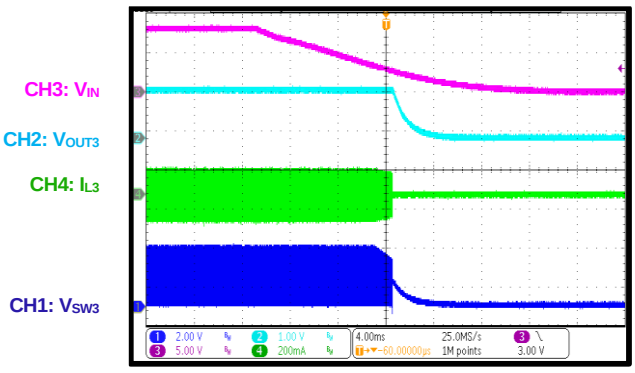
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 8V, V_{OUT1} = 3V, V_{OUT2} = 1.8V, V_{OUT3} = 1.2V, V_{LDO} = 2.5V, L1 = L2 = 2.2µH, L3 = 1µH, f_{SW1} = f_{SW2} = f_{SW3} = 2.2MHz, FCCM, T_A = 25°C, unless otherwise noted.

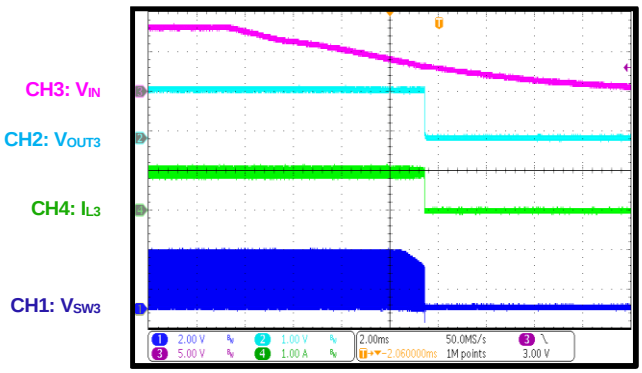
Shutdown through VIN (Buck 3)

I_{OUT1} = I_{OUT2} = I_{OUT3} = I_{LDO} = 0A



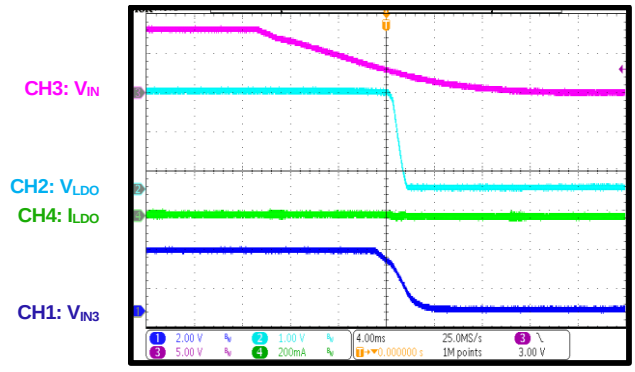
Shutdown through VIN (Buck 3)

I_{OUT1} = 0A, I_{OUT2} = 600mA, I_{OUT3} = 1A, I_{LDO} = 200mA



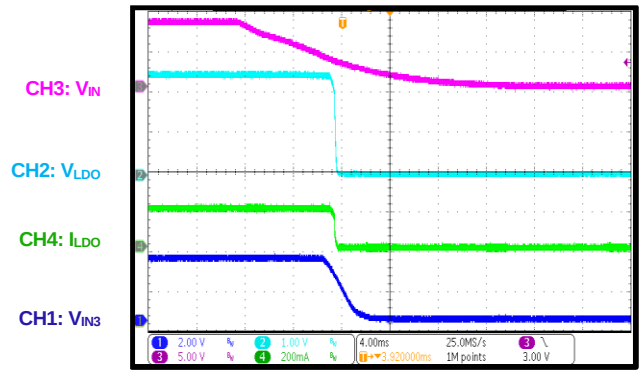
Shutdown through VIN (LDO)

I_{OUT1} = I_{OUT2} = I_{OUT3} = I_{LDO} = 0A

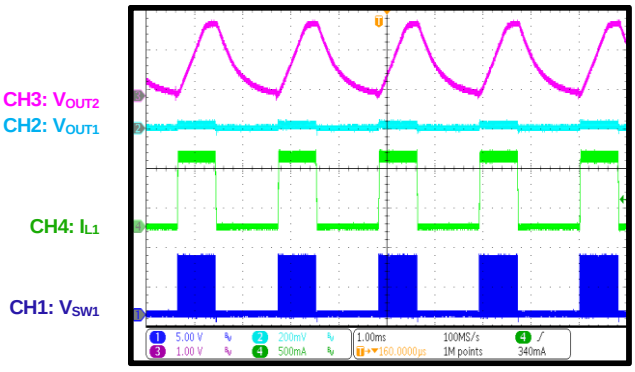


Shutdown through VIN (LDO)

I_{OUT1} = 0A, I_{OUT2} = 600mA, I_{OUT3} = 1A, I_{LDO} = 200mA

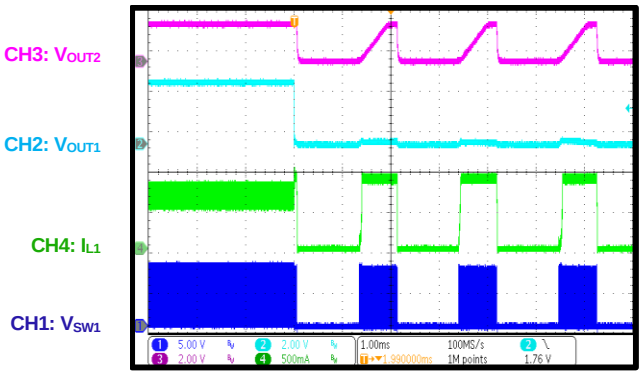


SCP Steady State (Buck 1)



SCP Entry (Buck 1)

I_{OUT1} = 0A, I_{OUT2} = 600mA, I_{OUT3} = 1A, I_{LDO} = 200mA



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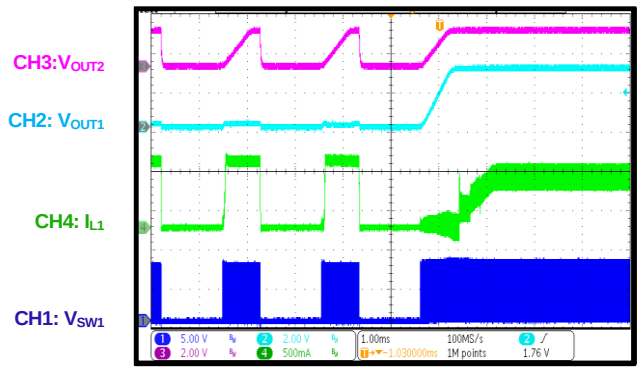
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

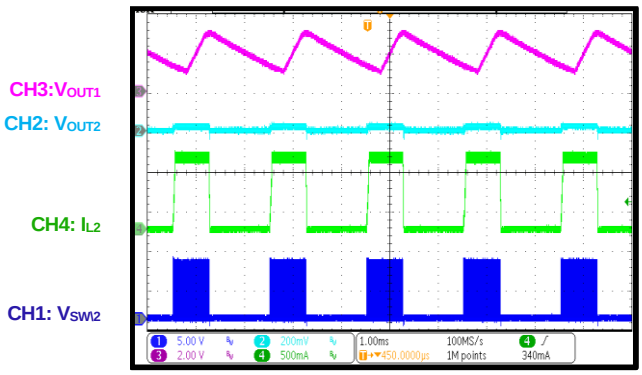
V_{IN} = 8V, V_{OUT1} = 3V, V_{OUT2} = 1.8V, V_{OUT3} = 1.2V, V_{LDO} = 2.5V, L1 = L2 = 2.2µH, L3 = 1µH, f_{SW1} = f_{SW2} = f_{SW3} = 2.2MHz, FCCM, T_A = 25°C, unless otherwise noted.

SCP Recovery (Buck 1)

I_{OUT1} = 0A, I_{OUT2} = 600mA, I_{OUT3} = 1A, I_{LDO} = 200mA

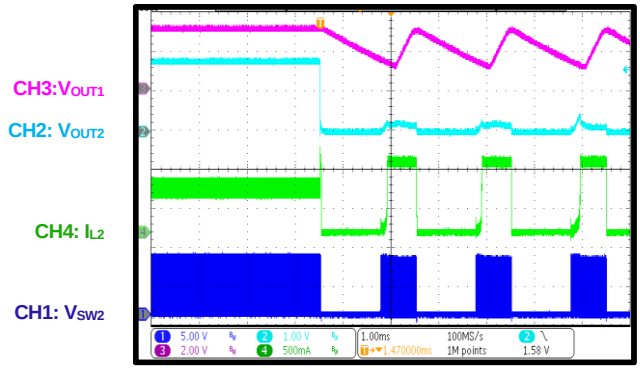


SCP Steady State (Buck 2)



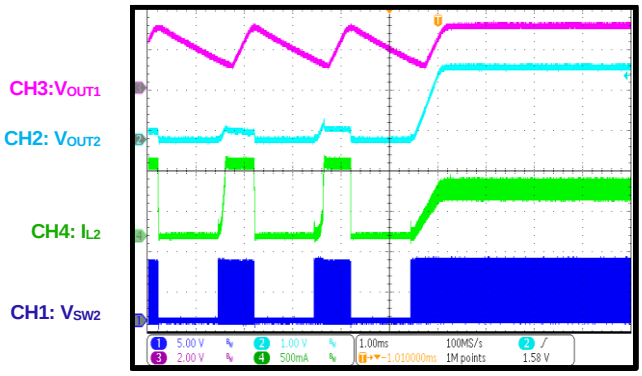
SCP Entry (Buck 2)

I_{OUT1} = 0A, I_{OUT2} = 600mA, I_{OUT3} = 1A, I_{LDO} = 200mA

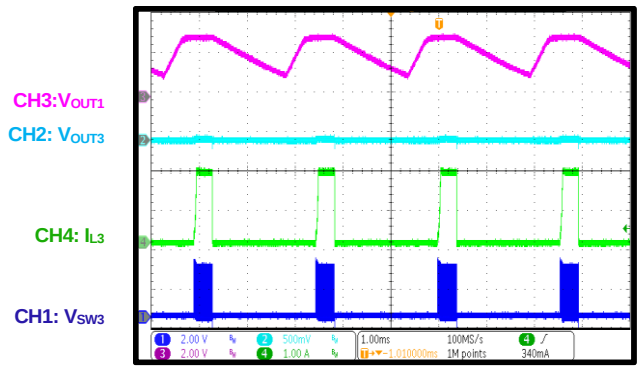


SCP Recovery (Buck 2)

I_{OUT1} = 0A, I_{OUT2} = 600mA, I_{OUT3} = 1A, I_{LDO} = 200mA

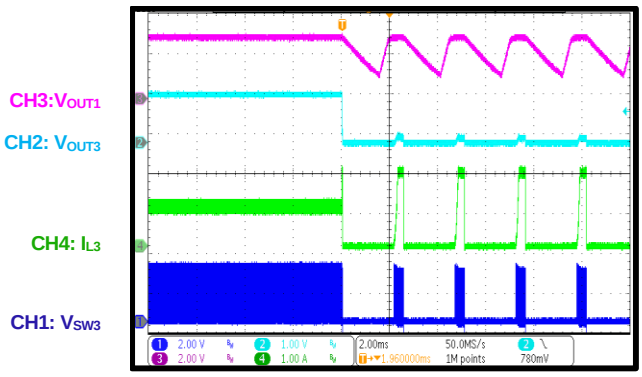


SCP Steady State (Buck 3)



SCP Entry (Buck 3)

I_{OUT1} = 0A, I_{OUT2} = 600mA, I_{OUT3} = 1A, I_{LDO} = 200mA



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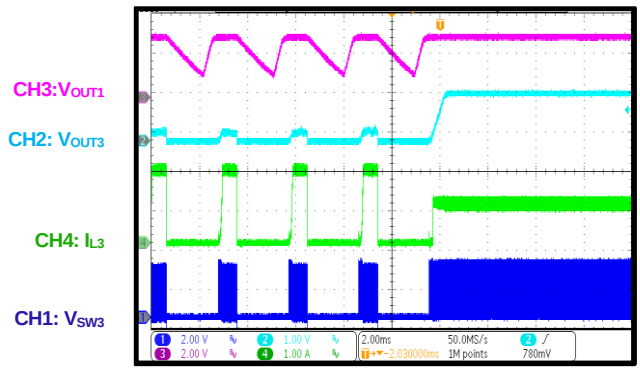
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

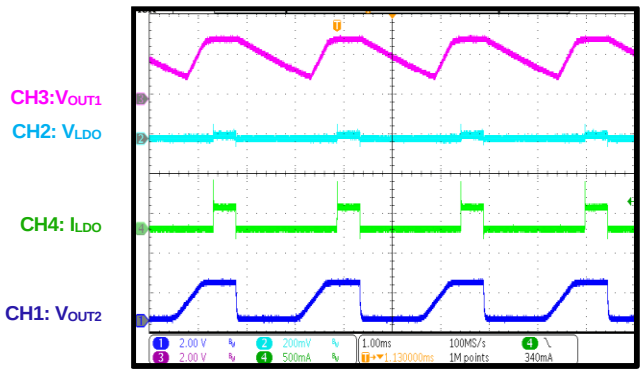
V_{IN} = 8V, V_{OUT1} = 3V, V_{OUT2} = 1.8V, V_{OUT3} = 1.2V, V_{LDO} = 2.5V, L1 = L2 = 2.2µH, L3 = 1µH, f_{SW1} = f_{SW2} = f_{SW3} = 2.2MHz, FCCM, T_A = 25°C, unless otherwise noted.

SCP Recovery (Buck 3)

I_{OUT1} = 0A, I_{OUT2} = 600mA, I_{OUT3} = 1A, I_{LDO} = 200mA

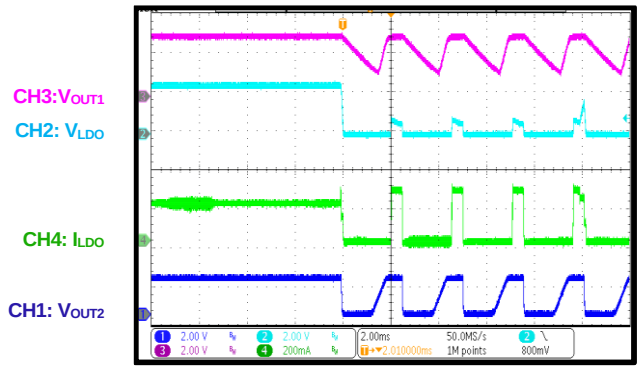


SCP Steady State (LDO)



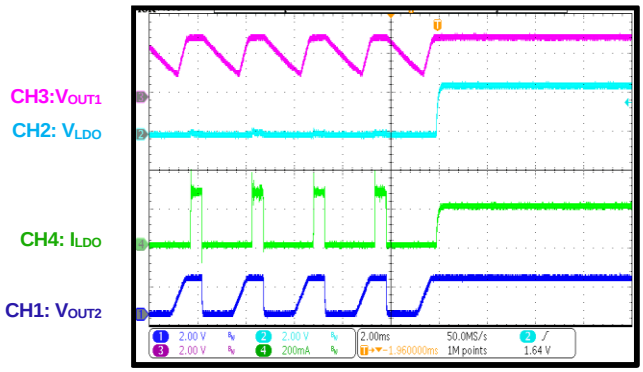
SCP Entry (LDO)

I_{OUT1} = 0A, I_{OUT2} = 600mA, I_{OUT3} = 1A, I_{LDO} = 200mA



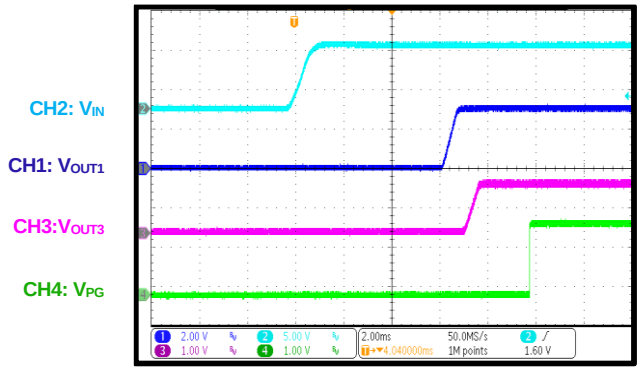
SCP Recovery (LDO)

I_{OUT1} = 0A, I_{OUT2} = 600mA, I_{OUT3} = 1A, I_{LDO} = 200mA



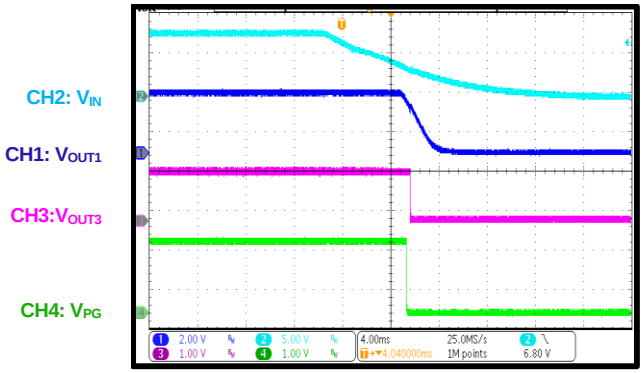
PG in Start-Up through VIN

I_{OUT1} = 0A, I_{OUT2} = 600mA, I_{OUT3} = 1A, I_{LDO} = 200mA



PG in Shutdown through VIN

I_{OUT1} = 0A, I_{OUT2} = 600mA, I_{OUT3} = 1A, I_{LDO} = 200mA



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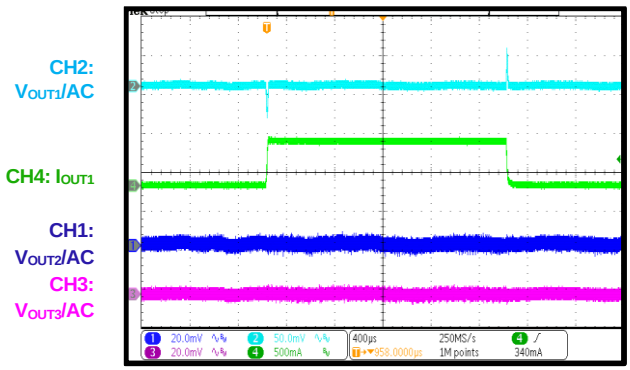
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 8V, V_{OUT1} = 3V, V_{OUT2} = 1.8V, V_{OUT3} = 1.2V, V_{LDO} = 2.5V, L1 = L2 = 2.2µH, L3 = 1µH, f_{SW1} = f_{SW2} = f_{SW3} = 2.2MHz, FCCM, T_A = 25°C, unless otherwise noted.

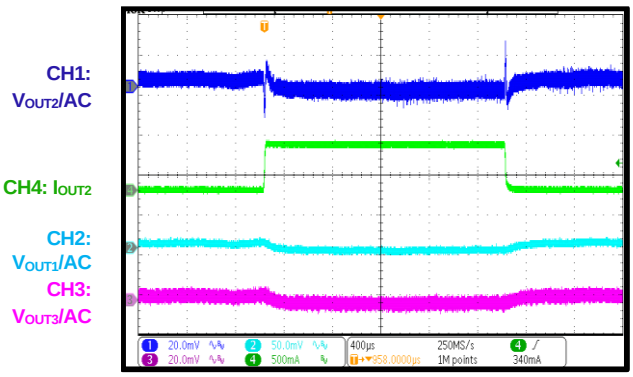
Load Transient Response (Buck 1)

I_{OUT1} = 0A to 600mA, I_{OUT2} = I_{OUT3} = I_{LDO} = 0A



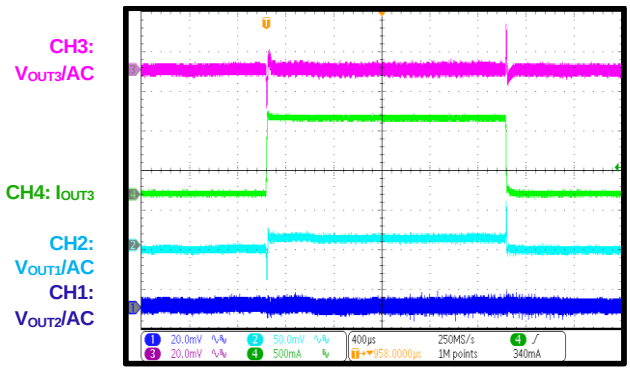
Load Transient Response (Buck 2)

I_{OUT1} = 0A, I_{OUT2} = 0A to 600mA, I_{OUT3} = 1A, I_{LDO} = 200mA



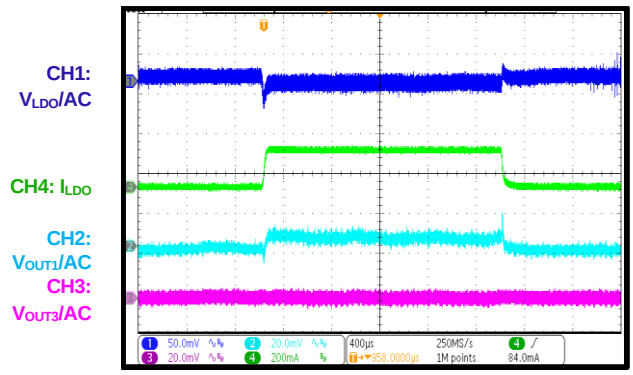
Load Transient Response (Buck 3)

I_{OUT1} = 0A, I_{OUT2} = 600mA, I_{OUT3} = 0A to 1A, I_{LDO} = 200mA



Load Transient Response (LDO)

I_{OUT1} = 0A, I_{OUT2} = 600mA, I_{OUT3} = 1A, I_{LDO} = 0mA to 200mA



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FUNCTIONAL BLOCK DIAGRAM

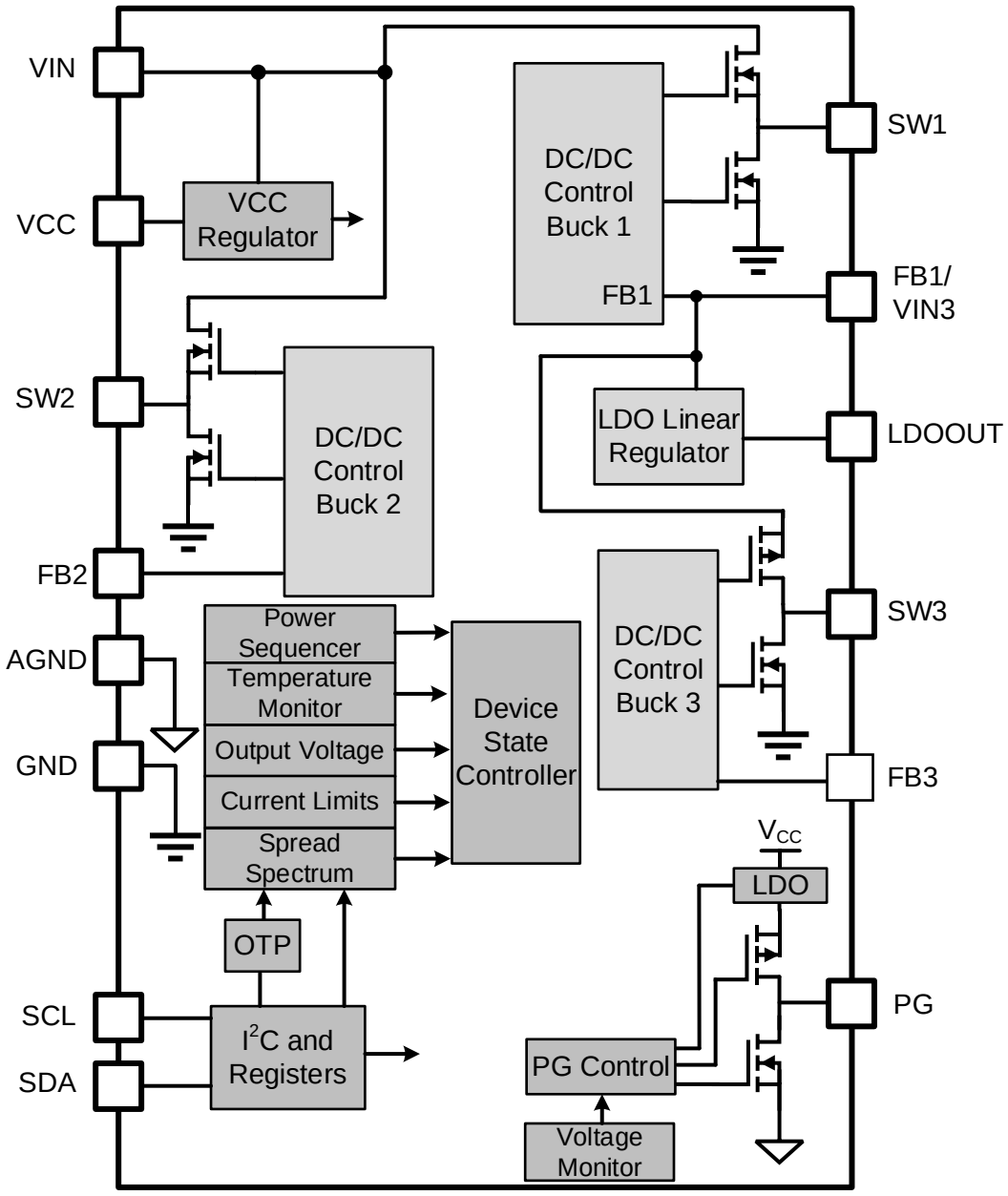

Figure 2: Functional Block Diagram

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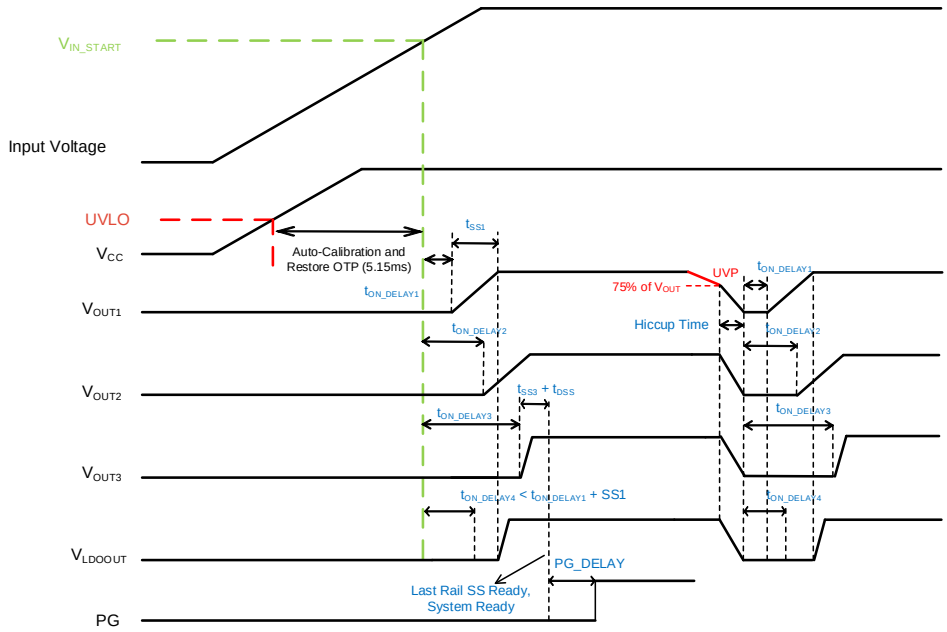
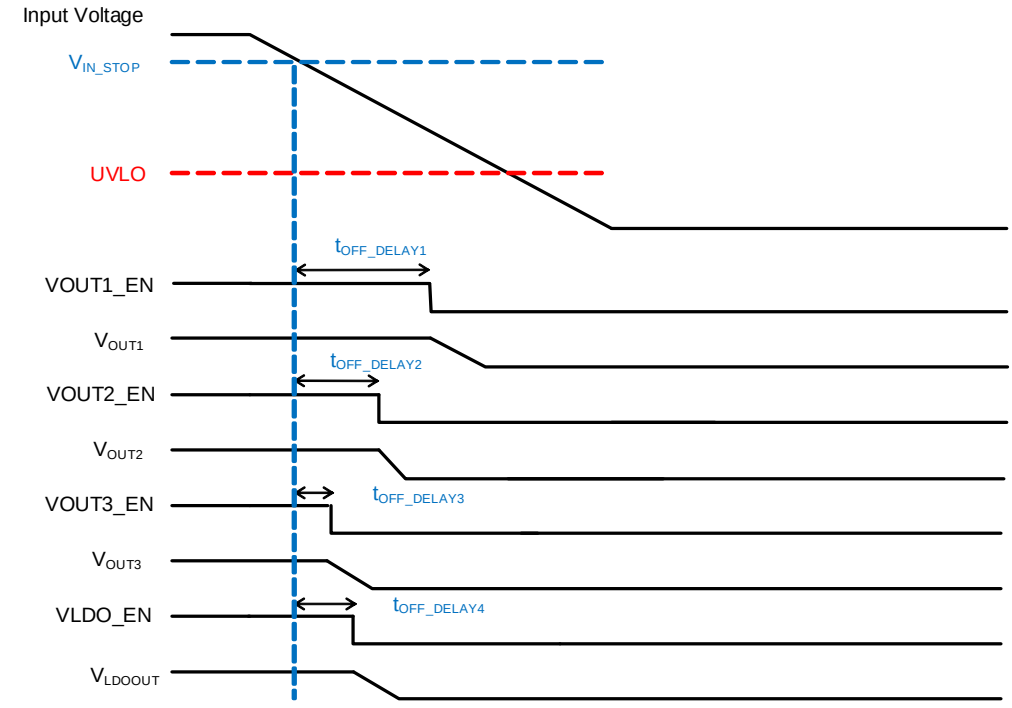
POWER-ON/OFF SEQUENCE



Notes:
1. If $V_{IN} > V_{IN_START}$ during the period of auto-calibration and restore OTP, the first channel will start after auto-calibration and restore OTP finishes.
2. If $t_{ON_DELAY1} + t_{SS1} > t_{ON_DELAY3}$ / t_{ON_DELAY4}, buck 3 and the LDO will begin to rise after V_{OUT1} is ready.

Figure 3: Power-On Sequence



Notes: The falling time will depend on the load.
If enabling output discharge, the pull-down resistor will turn on after VOUTX_EN falls until UVLO.

Figure 4: Power-Off Sequence

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OPERATION

The MPQ7928 provides a complete power management solution for automotive 8V systems, such as satellite cameras. It integrates three high-frequency, synchronous rectified, step-down, switch-mode converters and a low-dropout regulator. The MPQ7928 greatly reduces PCB size and component count with its compact QFN-15 (2.5mmx3.5mm) package.

The I²C interface provides adjustable default output voltage (V_{OUT}), power on sequence, and dynamic voltage scaling. It also provides powerful logic functions.

High-Efficiency Buck Regulators

Buck converter 1 (buck 1), buck converter 2 (buck 2), and buck converter 3 (buck 3) are synchronous, step-down DC/DC converters that have built-in under-voltage lockout (UVLO), soft start (SS), compensation, and current-limit protection with hiccup mode. Both buck 1 and buck 2 are medium-voltage (MV) bucks, and their input is the input voltage (V_{IN}). Buck 3 is a low-voltage (LV) buck and its input is buck 1's output.

Compared to fixed-frequency pulse-width modulation (PWM) control, constant on-time (COT) control offers a simpler control loop and faster transient response. Internal clock phase-locked loop (PLL) can ensure a fixed working frequency. When the low-side MOSFET (LS-FET) turns on, it remains on for at least as long as the minimum off time ($t_{MIN-OFF}$). Then the high-side MOSFET (HS-FET) turns on when the feedback voltage (V_{FB}) drops below the reference voltage (V_{REF}).

The switching clock is phase shifted from buck 1 to buck 2 during continuous conduction mode (CCM). Buck 1 is in phase with buck 3 during CCM.

LDOOUT

The MPQ7928 supports an adjustable-output and low-noise LDO output with over-voltage protection (OVP) and under-voltage protection (UVP). The LDO has an output that can be adjusted via the I²C interface, from 0.6V to 3.75V with 50mV/step. The LDO supports 200mA of output current (I_{LDO}) with over-current protection (OCP).

Power Supply and Under-Voltage Lockout (UVLO)

V_{IN} is the power supply for buck 1 and buck 2, and for the bias and internal logic blocks. VIN generates the VCC voltage (V_{CC}) through a regulator, and V_{CC} supplies power to each internal module. FB1/VIN3 is the feedback of buck 1, as well as the power supply for buck 3 and the LDO. If buck 1 is disabled via the digital interface, buck 3 and the LDO shut down.

When V_{IN} is below its UVLO threshold and V_{CC} exceeds its UVLO threshold, the MPQ7928 turns off all outputs (each channel turns off one by one according to the set shutdown sequence). If the output discharge function is enabled, the energy of the output capacitor (C_{OUT}) is released through the internal discharge path during shutdown.

When V_{CC} is below its UVLO threshold, the MPQ7928 turns off all outputs at the same time. During the shutdown process, the internal discharge path is not open, even if the output discharge function is enabled.

Internal Soft Start (SS)

Soft start (SS) is implemented to prevent the output voltage (V_{OUT}) from overshooting during start-up. When the MPQ7928 starts up, the internal circuitry of each power rail generates a soft-start voltage (V_{SS}) that ramps up from 0V. The soft-start time (t_{SS}) lasts until the voltage on the soft-start capacitor exceeds the reference voltage (V_{REF}). At this point, V_{REF} determines V_{OUT}. t_{SS} for each buck can be adjusted. The LDO's t_{SS} depends on the output capacitor (C_{OUT}) and output current (I_{OUT}) during start-up. See the Selecting the Output Capacitors (SW2, Pin 9; SW1, Pin 10; SW3, Pin 13; LDOOUT, Pin 15) section on page 64 to determine how to select the LDO capacitor.

Light-Load Operation

The MPQ7928 supports two light-load operation modes: continuous conduction mode (CCM) and discontinuous conduction mode (DCM).

In DCM, the inductor current (I_L) stays above 0A. After the HS-FET turns on for a calculated t_{ON}, the LS-FET turns on. The LS-FET stays on until I_L reaches the zero-current detection (ZCD)

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threshold. Then the LS-FET turns off and enters a high-impedance (Hi-Z) state. When V_{FB} drops below V_{REF}, the HS-FET turns on and stays on for the calculated t_{ON}.

In CCM, I_L can be negative, so the LS-FET can stay on even if I_L is below the ZCD threshold. After the HS-FET turns on for a calculated t_{ON}, the LS-FET turns on. When V_{FB} drops below V_{REF}, the LS-FET is off. Then the HS-FET turns on and stays on for the calculated t_{ON}.

Output Discharge

To discharge the energy of C_{OUT} during the power-off sequence, there is an active discharge path from the bucks and the LDO output to ground. The discharge path turns on when the corresponding channel is disabled. It is recommended to fully discharge all the outputs before beginning a new start-up sequence.

Power Good (PG)

The PG pin is a push-pull output that pulls logic high when the device is powered on, all outputs are within the PG range, and the fault registers are cleared. The high output level can be set to either 3.3V or 1.8V.

PG asserts if any of the below events occur:

- Buck 1's output is out of its V_{OUT} OVP/UVP threshold
- Buck 2's output is out of its PG range
- Buck 3's output is out of its PG range
- The LDO output is out of its PG range
- Thermal warning/thermal shutdown
- The LDO enters its dropout region
- Over-current (OC) failure
- $V_{IN} < V_{IN_STOP}$
- $V_{CC} < V_{CC_UVLO_FALLING}$
- I^2C communication failure
- I^2C CRC failure

If PG is pulled down because of these events, wait until the error is removed and all channels have finished starting, then wait for the PG de-assertion time before PG pulls up again. The PG de-assertion delay time is configurable.

Certain events can be masked (see Table 1). The PG_MAPPING register can determine whether PG is masked for these faults. See the PG_MAPPING (C5h) section on page 45 for more details.

Table 1: Maskable Fault Types

Fault Type	PG Asserts?	
	PG Masked	PG Not Masked
I^2C communication failure	No	Yes
I^2C CRC failure	No	Yes

For channels that are disabled in operation, PG does not indicate their output.

Over-Voltage Protection (OVP)

If any buck's output or the LDO output exceeds the over-voltage protection (OVP) threshold, all outputs shut down at the same time. The MPQ7928 stay off for a hiccup time. Then the normal start-up sequence starts again. If enabled, the output discharge function operates during the hiccup time.

Under-Voltage Protection (UVP)

If any buck's output or the LDO output falls below the under-voltage protection (UVP) threshold, all outputs shut down at the same time. The MPQ7928 stay off for a hiccup time. Then the normal start-up sequence starts again. If enabled, the output discharge function operates during the hiccup time.

Over-Current Protection (OCP)

For the three bucks, the MPQ7928 provides a peak/valley current limit (I_{LIMIT}) scheme designed to limit the peak/valley inductor current (I_L) to ensure that the switching currents remain within the device's capabilities during overload conditions or during an output short circuit.

When the HS-FET turns on, the device monitors the increased I_L through the relevant HS-FET. Once the peak I_L exceeds the peak I_{LIMIT}, the HS-FET turns off immediately, and the LS-FET turns on to conduct and decrease I_L. The HS-FET does not turn on again until I_L falls below the valley current limit threshold. If I_L exceeds the peak I_{LIMIT} during the minimum t_{ON} (t_{ON_MIN}), the HS-FET does not turn off immediately, and it does not turn off until the end of t_{ON_MIN}.

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If I_L does not fall below the valley I_{LIMIT} during the off time (the LS-FET turns on), or the peak I_L exceeds I_{LIMIT} during t_{ON} (HS-FET turns on) and lasts longer than the deglitch time, then an OC fault is recorded and OCP is triggered.

For the LDO, an internal, fixed current limit can ensure that the LDO's output current remains within the device's capabilities during overload conditions or during an output short circuit.

If any channel triggers an OC fault, all outputs shut down at the same time and stay off for the hiccup time. If enabled, the output discharge function operates during shutdown. Then the normal start-up sequence starts again with a configured turn-on delay. Bucks 1, 2, and 3 start according to the set t_{SS}, and the LDO determines the rising rate according to its load and capacitance. If no channel triggers OCP at the end of SS, then the MPQ7928 resumes normal operation.

Gate Drive Strength Control

To reduce electromagnetic interference (EMI), the MPQ7928 has four options set via GATE_DRIVE_STRENGTH to adjust the SW3 slew rate by adjusting the gate drive ability. EMI can be reduced with a slower SW3 slew rate, though this is a tradeoff that reduces efficiency.

Frequency Spread Spectrum (FSS)

To further optimize EMI performance, the MPQ7928 features frequency spread spectrum (FSS) (see Figure 5).

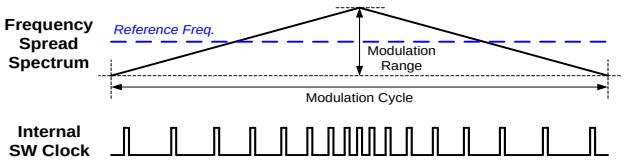

Figure 5: Frequency Spread Spectrum

The reference frequency and FSS modulation range can be set via the I²C interface.

Once FSS is enabled, the triangular frequency modulation mode varies the switching frequency (f_{SW}) between the same value exceeding or below the reference value. f_{SW} varies from the lowest value to its highest value, then drops back to the lowest value within a whole modulation cycle. See the FREQUENCY_DITHER (C4h) section on page 45 for the modulation cycle and range.

Thermal Warning and Shutdown

PG asserts low once the silicon die temperature exceeds its upper threshold (about 125°C) and de-asserts until the temperature drops below its lower threshold (about 105°C).

Thermal shutdown is implemented to protect the chip from thermal runaway. If the silicon die temperature exceeds its upper threshold (about 170°C), the device and power MOSFETs shut down. If the temperature drops below its lower threshold (about 150°C), the thermal shutdown condition is removed, and the chip is enabled again.

One-Time Programmable (OTP) Memory

The MPQ7928 provides a one-time programmable (OTP) memory function to set custom default parameters.

MPS provides a GUI and I²C tool to configure the MPQ7928 during the development process. Contact an MPS to configure in application.

Only the -0000 code (MPQ7928-0000 code) can be written to the OTP once. Other codes cannot be written to via the OTP. The OTP can be written to one time via a dedicated command. She the STORE_USER_ALL (15h) section on page 41 for more details.

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POWER CONTROL

Figure 6 shows several states of the MPQ7928 and the transition conditions between each state. The state machine's statuses are described below.

No Supply

The PMIC has a UVLO detection circuit. If V_{CC} is below its UVLO rising threshold, all of the MPQ7928's functions are disabled.

Power-Off

All power rails turn off. When V_{CC} exceeds its UVLO rising threshold and V_{IN} is below its starting voltage, the MPQ7928 enters a power off state. The digital block is reset, and the MPQ7928 executes auto-calibration.

After completing auto-calibration, the MPQ7928 begins to load its OTP data in the register. Before loading the OTP, if V_{IN} exceeds VIN_UVLO_RISING, the device generates a start signal after auto-calibration ends. After loading the OTP, if $V_{IN} > V_{IN_STOP}$, the device starts up and enters a power on sequence. If $V_{IN} < V_{IN_STOP}$ after loading the OTP finishes, the MPQ7928 stays in the power off state and does not start up.

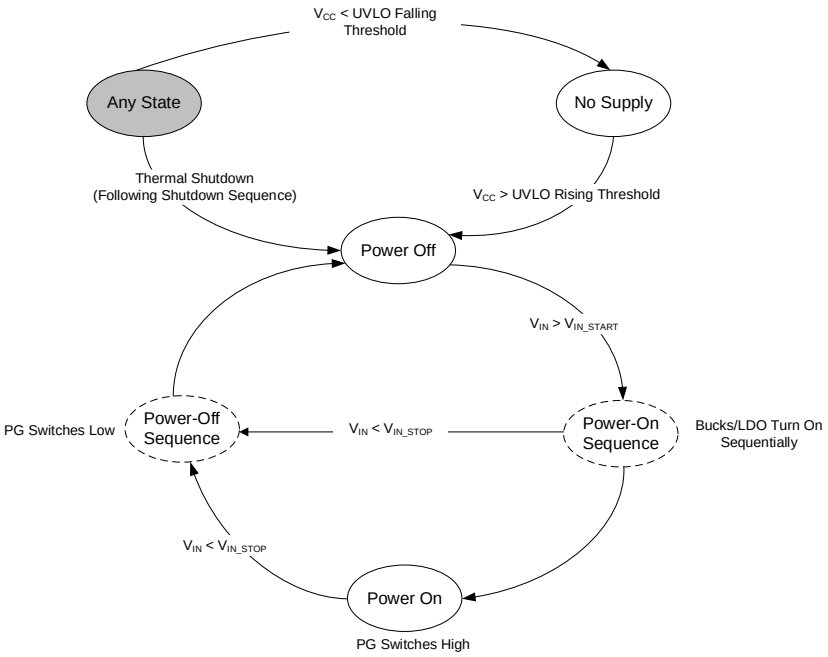

Figure 6: State Machine of the MPQ7928

Power-On Sequence

The start-up delay for the bucks and LDO can be configured via the OTP. Each output turns on after its configured delay. The bucks and the LDO turn on once their pre-configured on-time delay (ON_DELAY[7:4]) finishes. Buck 3 and the LDO must wait until buck 1 rises to its nominal output, then they begin to start up after a delay time.

The MPQ7928 has certain requirements for the start-up timing sequence.

- If t_{ON_DELAY2} - $t_{SSREDY1}$ > PG_DELAY, the PG signal pulls high after t_{SSREDY_1} + PG_DELAY, and pulls low again after t_{ON_DELAY2}.
- If t_{ON_DELAY3} - $t_{SSREDY2}$ > PG_DELAY, the PG signal pulls high after t_{SSREDY_2} + PG_DELAY, and pulls low again after t_{ON_DELAY3}.
- If t_{ON_DELAY4} - $t_{SSREDY3}$ > PG_DELAY, the PG signal pulls high after t_{SSREDY_3} + PG_DELAY, and pulls low again after t_{ON_DELAY4}.

Figure 7 on page 36 shows a diagram with the correct start-up timing.

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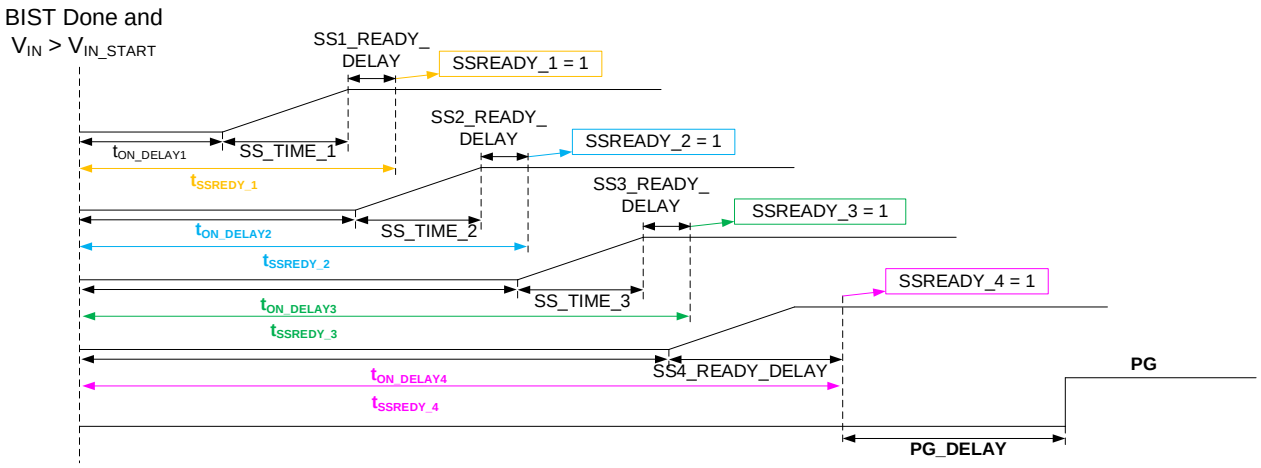

Figure 7: Power-On Sequence Diagram

Power-On

In this stage, the bucks and LDO are on. The PG pin switches high while the outputs are within their defined thresholds.

Power-Off Sequence

The device enters this sequence when it detects that V_{IN} < V_{IN_STOP} in a power on state, or during the power-on sequence period. The bucks and LDO turn off once the pre-configured off time delay (OFF_DELAY[3:0]) elapses for that output (see Figure 8).

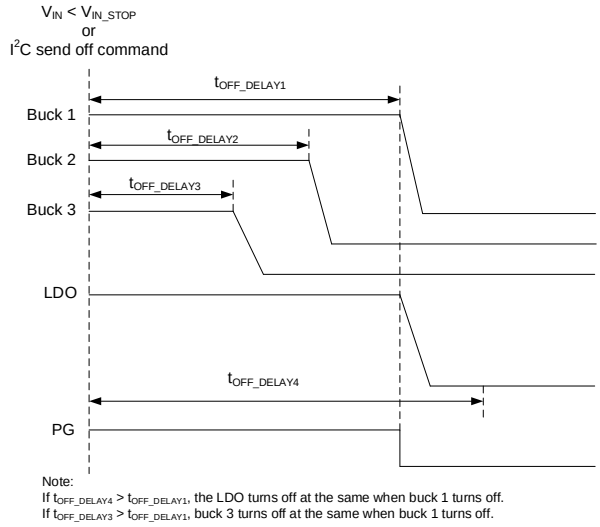

Figure 8: Power-Off Sequence Diagram

If a shutdown event occurs, the bucks and LDO turn off at the same time.

Shutdown Event

If the device detects a shutdown condition, it changes to the no supply or power-off state, regardless of the current state. Table 2 shows certain shutdown events.

Table 2: Shutdown Event

Fault Name	Result
V_{CC} < UVLO falling threshold	Enter a no supply state
Over-temperature (OT) fault	Enter a power-off state
V_{OUT} over-voltage (OV) fault	Enter a power-off state
V_{OUT} under-voltage (UV) fault	Enter a power-off state
Over-current (OC) fault	Enter a power-off state

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I²C INTERFACE

I²C Serial Interface Description

The power management bus (I²C) is an open-standard, power management protocol that defines a means of communication with power conversion and other devices. The I²C bus is a two-wire, bidirectional serial interface, consisting of a serial data line (SDA) and a serial clock line (SCL). The lines are externally pulled to a bus voltage when they are idle. Connecting to the line, a master device generates the SCL signal and device address, then arranges the communication sequence.

The MPQ7928 works as a slave-only device that supports both the standard mode (100kbps), fast mode (400kbps) and fast mode plus (1Mbps) bidirectional data transfer, adding flexibility to the power supply solution. The output voltage (V_{OUT}), transition slew rate, and other parameters can be instantaneously controlled via the I²C interface.

Data Validity

One clock pulse is generated for each data bit transferred. The data on the SDA line must be stable during the high period of the clock. The high or low state of the SDA line can only change when the clock signal on the SCL line is low (see Figure 9).

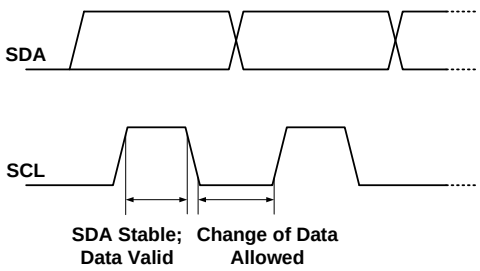

Figure 9: Bit Transfer

Start and Stop Commands

The start and stop commands are signaled by the master device, which signifies the beginning and the end of the I²C transfer. The start (S) command is defined as the SDA signal transitioning from high to low while the SCL line is high. The stop (P) command is defined as the SDA signal transitioning from low to high while the SCL is high (see Figure 10).

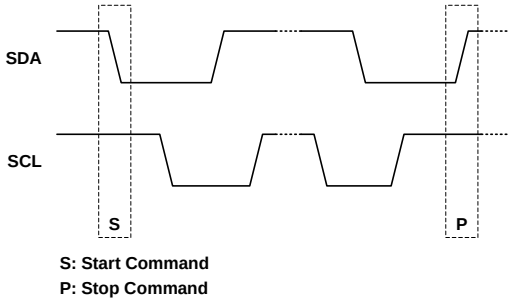

Figure 10: Start and Stop Commands

Start and stop commands are generated always by the master. The bus is considered busy after the start command. The bus is considered free again after a certain time after the stop command. The bus stays busy if a repeated start (Sr) command is generated instead of a stop command. The start and repeated start commands are functionally identical.

Transfer Data

Every byte put on the SDA line must be 8 bits long. Each byte must be followed by an acknowledge (ACK) bit. The acknowledge-related clock pulse is generated by the master. The transmitter releases the SDA line (high) during the acknowledge clock pulse. The receiver must pull down the SDA line during the acknowledge clock pulse, so that it remains stable low during the high period of the clock pulse.

Figure 11 shows the data transfer format . After the start command, a slave address is sent. This address is 7 bits long, followed by an 8th bit, which is a data direction bit (R/W). A “0’” indicates a transmission (write), while a “1” indicates a request for data (read). A data transfer is terminated always by a stop command, which is generated by the master. However, if a master still wishes to communicate on the bus, it can generate a repeated start command and address another slave without first generating a stop command.

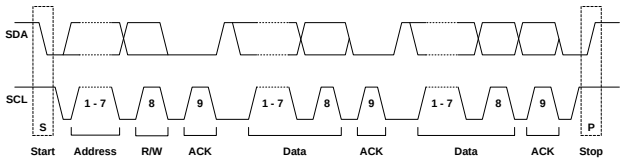

Figure 11: A Complete Data Transfer

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Packet Error Checking (PEC)

The packet error checking (PEC) mechanism is employed to improve communication reliability and robustness. When applicable, PEC is implemented by appending a packet error code after the data of each message transfer. The PEC is a CRC-8 error-checking byte ($C(x) = x^8 + x^2 + x^1 + 1$), calculated on all the message bytes (including addresses and read/write bits). The PEC is appended to the message by the device that supplied the last data byte.

If an incorrect PEC is received, a communications fault is triggered and the power good (PG) flag asserts until the fault register is cleared.

I²C Communication Failure

A data transmission fault occurs when the data is not properly transferred between the devices. There are several data transmission faults. All sorts of faults are listed below.

- Sending too little data
- Reading too little data
- The host sends too many bytes
- The host reads too many bytes
- Improperly set read bit in the address byte
- Unsupported command code

The communication failure is recorded in the STATUS_CML register.

Write/Read Sequence

All I²C commands are supported by MPQ7928 (see Figure 12 and Figure 13 on page 39). Five kinds of commands can be implemented with or without PEC:

1) Send command only
2) Write byte
3) Write word
4) Read byte
5) Read word

If the master writes a command to a read-only register, the MPQ7928 performs the same action as it would if the host sends too many bytes. If the master reads a command from a write-only register, the MPQ7928 performs the same action as it would if the host reads too many bytes.

Chip Address

The MPQ7928 supports 16 addresses, set via the ADDRESS register. The default 7-bit address is 03h.

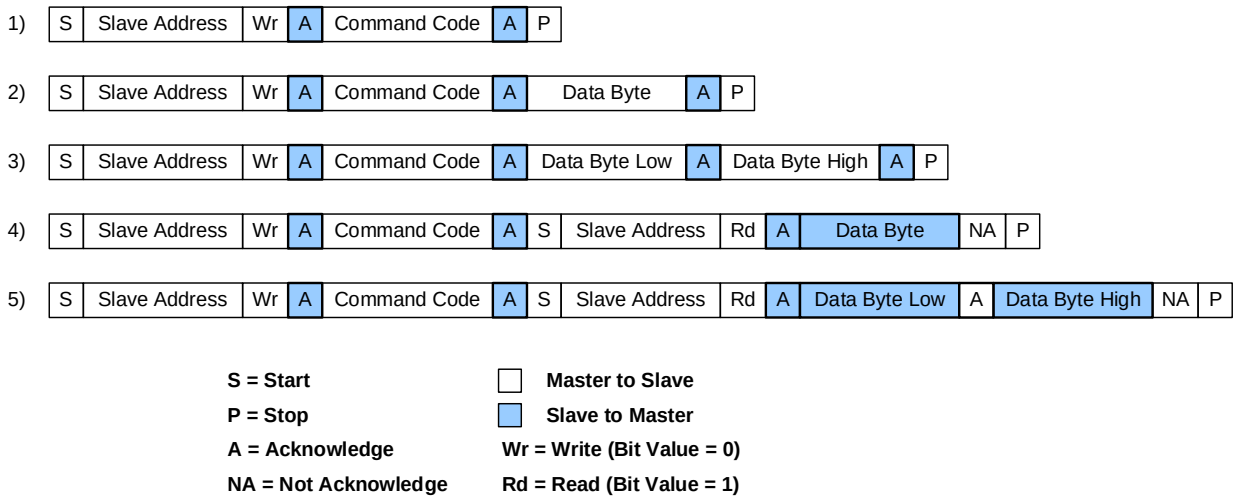

Figure 12: I²C Write/Read Sequence without PEC

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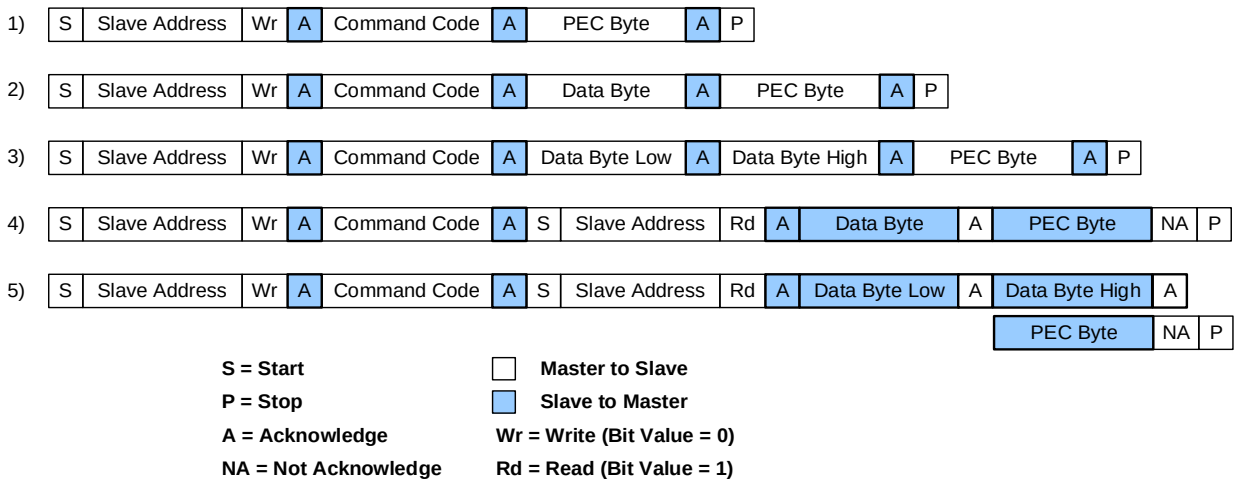

Figure 13: I²C Write/Read Sequence with PEC

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REGISTER MAP

Command Code	Command Name	Type	Bytes	Page 0 (Rail 1)	Page 1 (Rail 2)	Page 2 (Rail 3)	Page 3 (Rail 4)	Page FF (All Rails) (11)
00h	PAGE	R/W	1	✓	✓	✓	✓	✓ (12)
01h	OPERATION	R/W	1	✓	✓	✓	✓	✓
03h	CLEAR_FAULTS	Send	0	✓				✓
10h	WRITE_PROTECT	R/W	1	✓				✓
15h	STORE_USER_ALL	Send	0	✓				✓
16h	RESTORE_USER_ALL	Send	0	✓				✓
19h	CAPABILITY	R	1	✓				
20h	VOUT_MODE	R	1	✓				
21h	VOUT_COMMAND	R/W	2	✓	✓	✓	✓	✓
61h	TON_RISE	R/W	2	✓	✓	✓		✓
78h	STATUS_BYTE	R	1	✓	✓	✓	✓	
79h	STATUS_WORD	R	2	✓	✓	✓	✓	
7Ah	STATUS_VOUT	R	1	✓	✓	✓	✓	
7Bh	STATUS_IOUT	R	1	✓	✓	✓	✓	
7Dh	STATUS_TEMPERATURE	R	1	✓				
7Eh	STATUS_CML	R	1	✓				
80h	STATUS_MFR_SPECIFIC	R	1	✓				
C4h	FREQ_DITHER	R/W	1	✓				✓
C5h	PG_MAPPING	R/W	1	✓				✓
CBh	PROTECTION_CONFIG	R/W	1	✓				✓
CCh	PG_CONFIG	R/W	1	✓				✓
CDh	GATE_DRIVE_STRENGTH	R/W	1	✓				✓
CEh	LIGHT_LOAD	R/W	1	✓				✓
CFh	TON_OFF_DELAY	R/W	1	✓	✓	✓	✓	✓
D0h	TON_OFF_SCALE	R/W	1	✓				✓
D1h	FREQUENCY_ILIM_SCALE	R/W	1	✓				✓
D2h	VIN_START_STOP	R/W	1	✓				✓
D3h	ADDRESS	R/W	1	✓				✓
D4h	CONFIGURATION_CODE	R	1	✓				✓
D6h	LATEST_PEC	R	1	✓				✓

Notes:

11) A read command is invalid, but a write command is valid.
12) Read and write commands are valid.

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PAGE 0 REGISTER MAP

PAGE (00h)

Format: Unsigned binary

The PAGE command on Page 0 provides the ability to configure, control, and monitor all outputs through only one physical address. All subsequent commands that allow for multi-page actions are applied to the corresponding regulators selected by the PAGE (00h) command.

Bits	Access	Bit Name	Description
7:0	R/W	PAGE	8'b00000000: V_{OUT1} (Page 0) 8'b00000001: V_{OUT2} (Page 1) 8'b00000002: V_{OUT3} (Page 2) 8'b00000003: LDO (Page 3) 8'b11111111: All rails (Page FF) Others: Ineffective input

OPERATION (01h)

Format: Unsigned binary

The OPERATION command on Page 0 configures the on/off state for buck 1's output.

Bits	Access	Bit Name	Description
7	R/W	OPERATION	1'b1: The output is on 1'b0: The output is off
6:0	R/W	RESERVED	Reserved.

CLEAR_FAULTS (03h)

The CLEAR_FAULTS command on Page 0 clears any fault bits in the following status registers: STATUS_BYTE (78h), STATUS_WORD (79h), STATUS_VOUT (7Ah), STATUS_IOUT (7Bh), STATUS_INPUT (7Ch), STATUS_TEMPERATURE (7Dh), STATUS_CML (7Eh), and STATUS_MFR_SPECIFIC (80h).

This command is write-only. There is no data byte for this command.

WRITE_PROTECT (10h)

Format: Unsigned binary

The WRITE_PROTECT command on Page 0 controls writing to the converter. The intent of this command is to provide protection against accidental changes. It is not intended to provide protection against deliberate changes to the converter's configuration or operation. All the supported commands may have their parameters read, regardless of the WRITE_PROTECT settings.

Bits	Access	Bit Name	Description
7:0	R/W	WRITE_PROTECT	8'b10000000: Disable all writes except to the WRITE_PROTECT command 8'b 01000000: Disable all writes except to the WRITE_PROTECT, OPERATION, and PAGE commands 8'b 00100000: Disable all writes except to the WRITE_PROTECT, OPERATION, PAGE, and VOUT_COMMAND commands 8'b 00000000: Enable writes to all commands Others: Ineffective input

STORE_USER_ALL (15h)

The STORE_USER_ALL command on Page 0 instructs the MPQ7928 to copy the contents of the operating memory to the matching locations in the OTP, excluding the internal trim registers. This process occurs when MPQ70240FS receives a STORE_USER_ALL command from the digital interface.

This command is write-only. There is no data byte for this command.

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RESTORE_USER_ALL (16h)

The RESTORE_USER_ALL command on Page 0 instructs the MPQ7928 to copy the contents from the OTP and overwrite the matching locations in the operating memory, excluding the trim registers. Any items in the OTP that do not have matching locations in the operating memory are ignored.

The RESTORE_USER_ALL command can be used with the MPQ7928 is operating. However, the MPQ7928 may be unresponsive during the operation with unpredictable or undesirable results.

This command is write-only. There is no data byte for this command.

CAPABILITY (19h)

Format: Unsigned binary

The CAPABILITY command on Page 0 provides 1 byte to return the key digital interface features that the MPQ7928 can support.

Bits	Access	Bit Name	Description
7	R	PACKET_ERR_ CHECKING	1'b1: Packet error checking (PEC) is supported Others: Ineffective input
6:5	R	MAX_BUS_SPEED	2'b10: The maximum supported bus speed is 1MHz Others: Ineffective input
4	R	SMBALERT#	1'b0: The device does not have a SMBALERT# pin and does not support the SMBus alert response protocol Others: Ineffective input
3	R	NUMERIC_FORMAT	1'b0: Numeric data is in Linear11, ULinear16, SLinear16, or direct format Others: Ineffective input
2	R	AVSBUS_SUPPORT	1'b0: The AVSBus is not supported Others: Ineffective input
1:0	R	RESERVED	Reserved.

VOUT_MODE (20h)

Format: Unsigned binary

The VOUT_MODE command on Page 0 commands and reads the output voltage (V_{OUT}) mode. The 3MSB are used to determine the data format (only direct format is supported by the MPQ7928).

Bits	Access	Bit Name	Description
7:0	R	VOUT_MODE	8'b01000000: Direct mode. The coefficients are m = 2, R = 1, b = -1.2 Others: Ineffective input

VOUT_COMMAND (21h)

Format: Unsigned binary

The VOUT_COMMAND command on Page 0 sets buck 1's V_{OUT} (V_{OUT1}).

Bits	Access	Bit Name	Description
15:4	R/W	RESERVED	Reserved.
3:0	R/W	VOUT_CMD	V_{OUT1} can be calculated with the following equation: V_{OUT1} = VOUT_CMD x 100mV + 2.5V V_{OUT1} ranges between 2.5V and 4V. 100mV/step.

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TON_RISE (61h)

Format: Unsigned binary

The TON_RISE command on Page 0 sets buck 1's soft-start time (t_{SS_BUCK1}).

Bits	Access	Bit Name	Description
15:3	R/W	RESERVED	Reserved.
2:0	R/W	TON_RISE	t_{SS_BUCK1} can be calculated with the following equation: t_{SS_BUCK1} = (TON_RISE + 2) x 0.25ms t_{SS_BUCK1} ranges between 0.5ms and 2.25ms.

STATUS_BYTE (78h)

Format: Unsigned binary

The STATUS_BYTE command on Page 0 returns the value of certain flags that indicate the state of the MPQ7928.

Bits	Access	Bit Name	Description
7	R	BUSY	1'b0: No busy fault 1'b1: A fault was declared because the device was busy and unable to respond
6	R	OFF	1'b0: Device is on 1'b1: Device is off
5:3	R	RESERVED	Reserved.
2	R	TEMPERATURE	1'b0: No temperature fault or warning has occurred 1'b1: A temperature fault or warning has occurred
1	R	CML	1'b0: No communications, memory, or logic fault has occurred 1'b1: A communications, memory, or logic fault has occurred
0	R	FAULT_OTHER	1'b0: No other fault has occurred 1'b1: A fault not covered by bits[7:1] of this command has occurred

STATUS_WORD (79h)

Format: Unsigned binary

The STATUS_WORD command on Page 0 returns 2 bytes of information with a summary of the device's fault/warning conditions. The higher bytes return more detailed information of the fault conditions. The lower bytes are the same as what is returned by register STATUS_BYTE (78h).

Bits	Access	Bit Name	Description
15	R	VOUT_FAULT	1'b0: No V_{OUT} fault has occurred 1'b1: An V_{OUT} fault has occurred
14	R	IOUT_OC_FAULT	1'b0: No output current (I_{OUT}) fault has occurred 1'b1: An I_{OUT} fault has occurred
13	R	RESERVED	Reserved.
12	R	MANUFAC_FAULT	1'b0: No manufacturer-specific fault has occurred 1'b1: A manufacturer-specific fault has occurred
11	R	PGOOD	1'b0: PG is high 1'b1: PG is low
10:8	R	RESERVED	Reserved.
7:0	R	STATUS_BYTE	The same as STATUS BYTE (78h).

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STATUS_VOUT (7Ah)

Format: Unsigned binary

The STATUS_VOUT command on Page 0 returns the value of flags that indicate the device's V_{OUT} fault status.

Bits	Access	Bit Name	Description
7	R	VOUT_OV_FAULT	1'b0: No output over-voltage (OV) fault has occurred 1'b1: An output OV fault has occurred
6:5	R	RESERVED	Reserved.
4	R	VOUT_UV_FAULT	1'b0: No output under-voltage (UV) fault has occurred 1'b1: An output UV fault has occurred
3:0	R	RESERVED	Reserved.

STATUS_IOUT (7Bh)

Format: Unsigned binary

The STATUS_IOUT command on Page 0 returns the value of flags indicating the device's I_{OUT} fault status.

Bits	Access	Bit Name	Description
7	R	IOUT_OC_FAULT	1'b0: No output over-current (OC) fault has occurred 1'b1: An output OC fault has occurred
6:0	R	RESERVED	Reserved.

STATUS_TEMPERATURE (7Dh)

Format: Unsigned binary

The STATUS_TEMPERATURE command on Page 0 returns the value of flags that indicate the device's temperature fault status.

Bits	Access	Bit Name	Description
7	R	TEMP_OT_FAULT	1'b0: No over-temperature (OT) fault has occurred 1'b1: An OT fault has occurred
6	R	TEMP_OT_WARNING	1'b0: No OT warning has occurred 1'b1: An OT warning has occurred
5:0	R	RESERVED	Reserved.

STATUS_CML (7Eh)

Format: Unsigned binary

The STATUS_CML command on Page 0 returns the value of flags that indicate the device's communication fault status.

Bits	Access	Bit Name	Description
7	R	INVALID_CMD	1'b0: No invalid or unsupported commands have been received 1'b1: An invalid or unsupported command have been received
6	R	INVALID_DATA	1'b0: No invalid or unsupported data has been received 1'b1: Invalid or unsupported data has been received
5	R	PEC_ERROR	1'b0: The PEC has not failed 1'b1: The PEC has failed
4	R	CRC_ERROR	1'b0: The CRC has not failed 1'b1: The CRC has failed
3:0	R	RESERVED	Reserved.

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STATUS_MFR_SPECIFIC (80h)

Format: Unsigned binary

The STATUS_MFR_SPECIFIC command on Page 0 returns the value of flags indicating the PG over-voltage (OV) and under-voltage (UV) fault status.

Bits	Access	Bit Name	Description
7	R	RESERVED	Reserved.
6	R	PGOV_FAULT	1’b0: No PG OV fault has occurred in the buck 2, buck 3, or LDO channel 1’b1: A PG OV fault has occurred in the buck 2, buck 3, or LDO channel
5	R	PGUV_FAULT	1’b0: No PG UV fault has occurred in the buck 2, buck 3, or LDO channel 1’b1: A PG UV fault has occurred in the buck 2, buck 3, or LDO channel
4:0	R	RESERVED	Reserved.

FREQUENCY_DITHER (C4h)

Format: Unsigned binary

The FREQUENCY_DITHER command on Page 0 configures the frequency spread spectrum (FSS) parameters.

Bits	Access	Bit Name	Description
7	R/W	FSS_EN	Enables FSS control. 1’b0: Disabled 1’b1: Enabled
6:5	R/W	RESERVED	Reserved.
4	R/W	SSM_RAN	1’b0: ±5% spread spectrum modulation range 1’b1: ±10% spread spectrum modulation range
3:1	R/W	RESERVED	Reserved.
0	R/W	SSM_FRE	1’b0: 4.5kHz spread spectrum modulation frequency 1’b1: 9kHz spread spectrum modulation frequency

PG_MAPPING (C5h)

Format: Unsigned binary

The PG_MAPPING command on Page 0 configures PG mapping for certain faults.

Bits	Access	Bit Name	Description
7:4	R/W	RESERVED	Reserved.
3	R/W	PM_CML_PG#_ MAPPING	Sets the PG mapping for PMBus communication failures. 1’b0: A PMBus communication failure causes PG to go low and register assertion 1’b1: A PMBus communication failure causes register assertion only
2	R/W	PM_CRC_PG#_ MAPPING	Sets the PG mapping for PMBus CRC faults. 1’b0: A PMBus CRC failure causes PG to go low and register assertion 1’b1: A PMBus CRC failure causes register assertion only
1:0	R/W	RESERVED	Reserved.

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PROTECTION_CONFIG (CBh)

Format: Unsigned binary

The PROTECTION_CONFIG command on Page 0 enables packet error checking (PEC).

Bits	Access	Bit Name	Description
7:1	R/W	RESERVED	Reserved.
0	R/W	PEC_REQ	Indicates whether PEC is required. 1'b0: PEC is disabled 1'b1: PEC is optional

PG_CONFIG (CCh)

Format: Unsigned binary

The PG_CONFIG command on Page 0 configures the PG parameters.

Bits	Access	Bit Name	Description
7:4	R/W	RESERVED	Reserved.
3	R/W	PG_OUT	Sets the PG V_{OUT}. 1'b0: 1.8V 1'b1: 3.3V
2:1	R/W	PG_DELAY	Sets the PG de-assertion delay. 2'b00: Immediate 2'b01: 2ms 2'b10: 5ms 2'b11: 10ms
0	R/W	PG_THRESHOLD	Sets the PG threshold. 1'b0: ±4% 1'b1: ±6%

GATE_DRIVE STRENGTH (CDh)

Format: Unsigned binary

The GATE_DRIVE STRENGTH command on Page 0 configures the drive strength for buck 3's low-/high-side gate.

Bits	Access	Bit Name	Description
7:2	R/W	RESERVED	Reserved.
1:0	R/W	GATE_STR	2'b00: Low gate drive strength 2'b01: Medium-low gate drive strength 2'b10: Medium-high gate drive strength 2'b11: High gate drive strength

LIGHT_LOAD (CEh)

Format: Unsigned binary

The LIGHT_LOAD command on Page 0 configures the light-load operation mode and enables the output discharge function.

Bits	Access	Bit Name	Description
7:2	R/W	RESERVED	Reserved.
1	R/W	OUT_DIS	1'b0: Output discharge disabled 1'b1: Output discharge enabled

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0	R/W	LIGHT_MODE	1’b0: Continuous conduction mode (CCM) 1’b1: Discontinuous conduction mode (DCM)

TON_OFF_DELAY (CFh)

Format: Unsigned binary

The TON_OFF_DELAY command on Page 0 configures the turn-off and turn-on times.

Bits	Access	Bit Name	Description
7:4	R/W	ON_DELAY	Sets the turn-on delay, calculated with the following equation: Turn-On Delay = ON_DELAY x DELAY_SCALE Where DELAY_SCALE can range between 0ms and 3.75ms, or between 0ms and 37.5ms.
3:0	R/W	OFF_DELAY	Sets the turn-off delay, calculated with the following equation: Turn-Off Delay = OFF_DELAY x DELAY_SCALE Where DELAY_SCALE can range between 0ms and 3.75ms, or between 0ms and 37.5ms.

TON_OFF_SCALE (D0h)

Format: Unsigned binary

The TON_OFF_SCALE command on Page 0 configures the scale for the turn-off and turn-on times.

Bits	Access	Bit Name	Description
7:1	R/W	RESERVED	Reserved.
0	R/W	DELAY_SCALE	Sets the delay scale. 1’b0: Scale = 0.25ms. The delay ranges between 0ms and 3.75ms 1’b1: Scale = 2.5ms. The delay ranges between 0ms and 37.5ms

FREQUENCY_ILIM_SCALE (D1h)

Format: Unsigned binary

The FREQUENCY_ILIM_SCALE command on Page 0 configures the switching frequency (f_{SW}) and current limit (I_{LIMIT}) for buck 1, buck 2, and buck 3.

Bits	Access	Bit Name	Description
7:2	R/W	RESERVED	Reserved.
1	R/W	FREQUENCY	Sets f_{SW} for buck 1, buck 2, and buck 3. 1’b0: 2.2MHz 1’b1: 3.3MHz
0	R/W	ILIM	Sets I_{LIMIT} for buck 1, buck 2, and buck 3. 1’b0: 100% of the current limit 1’b1: 125% of the current limit

VIN_START_STOP (D2h)

Format: Unsigned binary

The VIN_START_STOP command on Page 0 configures the start voltage for VIN (V_{IN_START}) and stop voltage for VIN (V_{IN_STOP}). To modify this register, V_{IN_START} and V_{IN_STOP} must both be set to the under-voltage lockout (UVLO) threshold, or they must both be set to other values.

Bits	Access	Bit Name	Description
7:4	R/W	RESERVED	Reserved.

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3:2	R/W	VIN_START	Sets V_{IN_START}. 2'b00: UVLO threshold 2'b01: 4V 2'b10: 5V 2'b11: 6V
1:0	R/W	VIN_STOP	Sets V_{IN_STOP}. 2'b00: UVLO threshold 2'b01: 3.5V 2'b10: 4.5V 2'b11: 5.5V

ADDRESS (D3h)

Format: Unsigned binary

The ADDRESS command on Page 0 sets the digital interface communication address.

Bits	Access	Bit Name	Description
7:4	R/W	RESERVED	Reserved.
3:0	R/W	ADDRESS	Sets the 4 bits of the digital interface address.

CONFIGURATION_CODE (D4h)

Format: Unsigned binary

The CONFIGURATION_CODE command on Page 0 returns information regarding the configuration code.

Bits	Access	Bit Name	Description
7:4	R	RESERVED	Reserved.
3:0	R	CONFIG_CODE	Sets the OTP configuration code at shipment.

LATEST_PEC (D6h)

Format: Unsigned binary

The LATEST_PEC command on Page 0 stores the latest calculated packet error code from the previous write transition.

Bits	Access	Bit Name	Description
7:0	R	LATEST_PEC	Stores the latest calculated packet error code from the previous write transition.

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PAGE 1 REGISTER MAP

PAGE (00h)

Format: Unsigned binary

The PAGE command on Page 1 provides the ability to configure, control, and monitor all outputs through only one physical address. All subsequent commands that allow for multi-page actions are applied to the corresponding regulators selected by the PAGE (00h) command.

Bits	Access	Bit Name	Description
7:0	R/W	PAGE	8'b00000000: V_{OUT1} (Page 0) 8'b00000001: V_{OUT2} (Page 1) 8'b00000002: V_{OUT3} (Page 2) 8'b00000003: LDO (Page 3) 8'b11111111: All rails (Page FF) Others: Ineffective input

OPERATION (01h)

Format: Unsigned binary

The OPERATION command on Page 1 configures the on/off state for buck 2's output.

Bits	Access	Bit Name	Description
7	R/W	OPERATION	1'b1: The output is on 1'b0: The output is off
6:0	R/W	RESERVED	Reserved.

VOUT_COMMAND (21h)

Format: Unsigned binary

The VOUT_COMMAND command Page 1 sets buck 2's output voltage (V_{OUT2}).

Bits	Access	Bit Name	Description
15:6	R/W	RESERVED	Reserved.
5:0	R/W	VOUT_CMD	V_{OUT2} can be calculated with the following equation: V_{OUT2} = VOUT_CMD x 50mV + 0.6V V_{OUT2} ranges between 0.6V and 3.75V. 50mV/step.

TON_RISE (61h)

Format: Unsigned binary

The TON_RISE command on Page 1 sets buck 2's soft-start time (t_{SS_BUCK2}).

Bits	Access	Bit Name	Description
15:3	R/W	RESERVED	Reserved.
2:0	R/W	TON_RISE	t_{SS_BUCK2} can be calculated with the following equation: t_{SS_BUCK2} = (TON_RISE + 2) x 0.25ms t_{SS_BUCK2} ranges between 0.5ms and 2.25ms.

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STATUS_BYTE (78h)

Format: Unsigned binary

The STATUS_BYTE command on Page 1 returns the value of flags that indicate the state of the MPQ7928.

Bits	Access	Bit Name	Description
7	R	BUSY	1'b0: No busy fault 1'b1: A fault was declared because the device was busy and unable to respond
6	R	OFF	1'b0: Device is on 1'b1: Device is off
5:3	R	RESERVED	Reserved.
2	R	TEMPERATURE	1'b0: No temperature fault or warning has occurred 1'b1: A temperature fault or warning has occurred
1	R	CML	1'b0: No communications, memory, or logic fault has occurred 1'b1: A communications, memory, or logic fault has occurred
0	R	FAULT_OTHER	1'b0: No other fault has occurred 1'b1: A fault not covered by bits[7:1] of this command has occurred

STATUS_WORD (79h)

Format: Unsigned binary

The STATUS_WORD command on Page 1 returns 2 bytes of information with a summary of the device's fault/warning conditions. The higher bytes return more detailed information of the fault conditions. The lower bytes are the same as what is returned by register STATUS_BYTE (78h).

Bits	Access	Bit Name	Description
15	R	VOUT_FAULT	1'b0: No output voltage (V_{OUT}) fault has occurred 1'b1: An V_{OUT} fault has occurred
14	R	IOUT_OC_FAULT	1'b0: No output current (I_{OUT}) fault has occurred 1'b1: An I_{OUT} fault has occurred
13	R	RESERVED	Reserved.
12	R	MANUFAC_FAULT	1'b0: No manufacturer-specific fault has occurred 1'b1: A manufacturer-specific fault has occurred
11	R	PGOOD	1'b0: PG is high 1'b1: PG is low
10:8	R	RESERVED	Reserved.
7:0	R	STATUS_BYTE	The same as STATUS BYTE (78h).

STATUS_VOUT (7Ah)

Format: Unsigned binary

The STATUS_VOUT command on Page 1 returns the value of flags that indicate the device's V_{OUT} fault status.

Bits	Access	Bit Name	Description
7	R	VOUT_OV_FAULT	1'b0: No output over-voltage (OV) fault has occurred 1'b1: An output OV fault has occurred
6:5	R	RESERVED	Reserved.

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4	R	VOUT_UV_FAULT	1’b0: No output under-voltage (UV) fault has occurred 1’b1: An output UV fault has occurred
3:0	R	RESERVED	Reserved.

STATUS_IOUT (7Bh)

Format: Unsigned binary

The STATUS_IOUT command on Page 1 returns the value of flags indicating the device’s I_{OUT} fault status.

Bits	Access	Bit Name	Description
7	R	IOUT_OC_FAULT	1’b0: No output over-current (OC) fault has occurred 1’b1: An output OC fault has occurred
6:0	R	RESERVED	Reserved.

TON_OFF_DELAY (CFh)

Format: Unsigned binary

The TON_OFF_DELAY command on Page 1 configures buck 2’s turn-off and turn-on times.

Bits	Access	Bit Name	Description
7:4	R/W	ON_DELAY	Sets the turn-on delay, calculated with the following equation: Turn-On Delay = ON_DELAY x DELAY_SCALE Where DELAY_SCALE can range between 0ms and 3.75ms, or between 0ms and 37.5ms.
3:0	R/W	OFF_DELAY	Sets the turn-off delay, calculated with the following equation: Turn-Off Delay = OFF_DELAY x DELAY_SCALE Where DELAY_SCALE can range between 0ms and 3.75ms, or between 0ms and 37.5ms.

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PAGE 2 REGISTER MAP

PAGE (00h)

Format: Unsigned binary

The PAGE command on Page 2 provides the ability to configure, control, and monitor all outputs through only one physical address. All subsequent commands that allow for multi-page actions are applied to the corresponding regulators selected by the PAGE (00h) command.

Bits	Access	Bit Name	Description
7:0	R/W	PAGE	8'b00000000: V_{OUT1} (Page 0) 8'b00000001: V_{OUT2} (Page 1) 8'b00000002: V_{OUT3} (Page 2) 8'b00000003: LDO (Page 3) 8'b11111111: All rails (Page FF) Others: Ineffective input

OPERATION (01h)

Format: Unsigned binary

The OPERATION command on Page 2 configures the on/off state for buck 3's output.

Bits	Access	Bit Name	Description
7	R/W	OPERATION	1'b1: The output is on 1'b0: The output is off
6:0	R/W	RESERVED	Reserved.

VOUT_COMMAND (21h)

Format: Unsigned binary

The VOUT_COMMAND command on Page 2 sets buck 3's output voltage (V_{OUT3}).

Bits	Access	Bit Name	Description
15:6	R/W	RESERVED	Reserved.
5:0	R/W	VOUT_CMD	V_{OUT3} can be calculated with the following equation: V_{OUT3} = VOUT_CMD x 50mV + 0.6V V_{OUT3} ranges between 0.6V and 2.55V. This value is clamped to 2.55V when V_{OUT3} is set to exceed 2.55V. 50mV/step.

TON_RISE (61h)

Format: Unsigned binary

The TON_RISE command on Page 2 sets buck 3's soft-start time (t_{SS_BUCK3}).

Bits	Access	Bit Name	Description
15:3	R/W	RESERVED	Reserved.
2:0	R/W	TON_RISE	t_{SS_BUCK3} can be calculated with the following equation: t_{SS_BUCK3} = (TON_RISE + 2) x 0.25ms t_{SS_BUCK3} ranges between 0.5ms and 2.25ms.

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STATUS_BYTE (78h)

Format: Unsigned binary

The STATUS_BYTE command on Page 2 returns the value of flags that indicate the state of the MPQ7928.

Bits	Access	Bit Name	Description
7	R	BUSY	1'b0: No busy fault 1'b1: A fault was declared because the device was busy and unable to respond
6	R	OFF	1'b0: Device is on 1'b1: Device is off
5:3	R	RESERVED	Reserved.
2	R	TEMPERATURE	1'b0: No temperature fault or warning has occurred 1'b1: A temperature fault or warning has occurred
1	R	CML	1'b0: No communications, memory, or logic fault has occurred 1'b1: A communications, memory, or logic fault has occurred
0	R	FAULT_OTHER	1'b0: No other fault has occurred 1'b1: A fault not covered by bits[7:1] of this command has occurred

STATUS_WORD (79h)

Format: Unsigned binary

The STATUS_WORD command on Page 2 returns 2 bytes of information with a summary of the device's fault/warning conditions. The higher bytes return more detailed information of the fault conditions. The lower bytes are the same as what is returned by register STATUS_BYTE (78h).

Bits	Access	Bit Name	Description
15	R	VOUT_FAULT	1'b0: No output voltage (V_{OUT}) fault has occurred 1'b1: An V_{OUT} fault has occurred
14	R	IOUT_OC_FAULT	1'b0: No output current (I_{OUT}) fault has occurred 1'b1: An I_{OUT} fault has occurred
13	R	RESERVED	Reserved.
12	R	MANUFAC_FAULT	1'b0: No manufacturer-specific fault has occurred 1'b1: A manufacturer-specific fault has occurred
11	R	PGOOD	1'b0: PG is high 1'b1: PG is low
10:8	R	RESERVED	Reserved.
7:0	R	STATUS_BYTE	The same as STATUS BYTE (78h).

STATUS_VOUT (7Ah)

Format: Unsigned binary

The STATUS_VOUT command on Page 2 returns the value of flags that indicate the device's V_{OUT} fault status.

Bits	Access	Bit Name	Description
7	R	VOUT_OV_FAULT	1'b0: No output over-voltage (OV) fault has occurred 1'b1: An output OV fault has occurred
6:5	R	RESERVED	Reserved.

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4	R	VOUT_UV_FAULT	1’b0: No output under-voltage (UV) fault has occurred 1’b1: An output UV fault has occurred
3:0	R	RESERVED	Reserved.

STATUS_IOUT (7Bh)

Format: Unsigned binary

The STATUS_IOUT command on Page 2 returns the value of flags indicating the device’s I_{OUT} fault status.

Bits	Access	Bit Name	Description
7	R	IOUT_OC_FAULT	1’b0: No output over-current (OC) fault has occurred 1’b1: An output OC fault has occurred
6:0	R	RESERVED	Reserved.

TON_OFF_DELAY (CFh)

Format: Unsigned binary

The TON_OFF_DELAY command on Page 2 configures buck 3’s turn-off and turn-on times.

Bits	Access	Bit Name	Description
7:4	R/W	ON_DELAY	Sets the turn-on delay, calculated with the following equation: Turn-On Delay = ON_DELAY x DELAY_SCALE Where DELAY_SCALE can range between 0ms and 3.75, or between 0ms and 37.5ms.
3:0	R/W	OFF_DELAY	Sets the turn-off delay, calculated with the following equation: Turn-Off Delay = OFF_DELAY x DELAY_SCALE Where DELAY_SCALE can range between 0ms and 3.75, or between 0ms and 37.5ms.

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PAGE 3 REGISTER MAP

PAGE (00h)

Format: Unsigned binary

The PAGE command on Page 3 provides the ability to configure, control, and monitor all outputs through only one physical address. All subsequent commands that allow for multi-page actions are applied to the corresponding regulators selected by the PAGE (00h) command.

Bits	Access	Bit Name	Description
7:0	R/W	PAGE	8'b00000000: V_{OUT1} (Page 0) 8'b00000001: V_{OUT2} (Page 1) 8'b00000002: V_{OUT3} (Page 2) 8'b00000003: LDO (Page 3) 8'b11111111: All rails (Page FF) Others: Ineffective input

OPERATION (01h)

Format: Unsigned binary

The OPERATION command on Page 3 is used to configures the on/off state for the LDO's output.

Bits	Access	Bit Name	Description
7	R/W	OPERATION	1'b1: Output on 1'b0: Output off
6:0	R/W	RESERVED	Reserved.

VOUT_COMMAND (21h)

Format: Unsigned binary

The VOUT_COMMAND command on Page 3 sets the LDO's output voltage (V_{LDO}).

Bits	Access	Bit Name	Description
15:6	R/W	RESERVED	Reserved.
5:0	R/W	VOUT_CMD	V_{LDO} can be calculated with the following equation: V_{LDO} = VOUT_CMD x 50mV + 0.6V V_{LDO} ranges between 0.6V and 3.75V. 50mV/step.

STATUS_BYTE (78h)

Format: Unsigned binary

The STATUS_BYTE command on Page 3 returns the value of flags that indicate the state of the MPQ7928.

Bits	Access	Bit Name	Description
7	R	BUSY	1'b0: No busy fault 1'b1: A fault was declared because the device was busy and unable to respond
6	R	OFF	1'b0: Device is on 1'b1: Device is off
5:3	R	RESERVED	Reserved.
2	R	TEMPERATURE	1'b0: No temperature fault or warning has occurred 1'b1: A temperature fault or warning has occurred
1	R	CML	1'b0: No communications, memory, or logic fault has occurred 1'b1: A communications, memory, or logic fault has occurred

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0	R	FAULT_OTHER	1’b0: No other fault has occurred 1’b1: A fault not covered by bits[7:1] of this command has occurred

STATUS_WORD (79h)

Format: Unsigned binary

The STATUS_WORD command on Page 3 returns 2 bytes of information with a summary of the device’s fault/warning conditions. The higher bytes return more detailed information of the fault conditions. The lower bytes are the same as what is returned by register STATUS_BYTE (78h).

Bits	Access	Bit Name	Description
15	R	VOUT_FAULT	1’b0: No output voltage (V_{OUT}) fault has occurred 1’b1: An V_{OUT} fault has occurred
14	R	IOUT_OC_FAULT	1’b0: No output current (I_{OUT}) fault has occurred 1’b1: An I_{OUT} fault has occurred
13	R	RESERVED	Reserved.
12	R	MANUFAC_FAULT	1’b0: No manufacturer-specific fault has occurred 1’b1: A manufacturer-specific fault has occurred
11	R	PGOOD	1’b0: PG is high 1’b1: PG is low
10:8	R	RESERVED	Reserved.
7:0	R	STATUS_BYTE	The same as STATUS BYTE (78h).

STATUS_VOUT (7Ah)

Format: Unsigned binary

The STATUS_VOUT command on Page 3 returns the value of flags that indicate the device’s V_{OUT} fault status.

Bits	Access	Bit Name	Description
7	R	VOUT_OV_FAULT	1’b0: No output over voltage fault has occurred 1’b1: An output over voltage fault has occurred
6:5	R	RESERVED	Reserved.
4	R	VOUT_UV_FAULT	1’b0: No output under voltage fault has occurred 1’b1: An output under voltage fault has occurred
3:0	R	RESERVED	Reserved.

STATUS_IOUT (7Bh)

Format: Unsigned binary

The STATUS_IOUT command on Page 3 returns the value of flags indicating the device’s I_{OUT} fault status.

Bits	Access	Bit Name	Description
7	R	IOUT_OC_FAULT	1’b0: No output over-current (OC) fault has occurred 1’b1: An output OC fault has occurred
6:0	R	RESERVED	Reserved.

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TON_OFF_DELAY (CFh)

Format: Unsigned binary

The TON_OFF_DELAY command on Page 3 configures the turn-off and turn-on times for the LDO.

Bits	Access	Bit Name	Description
7:4	R/W	ON_DELAY	Sets the turn-on delay, calculated with the following equation: Turn-On Delay = ON_DELAY x DELAY_SCALE Where DELAY_SCALE can range between 0ms and 3.75ms, or between 0ms and 37.5ms.
3:0	R/W	OFF_DELAY	Sets the turn-off delay, calculated with the following equation: Turn-Off Delay = OFF_DELAY x DELAY_SCALE Where DELAY_SCALE can range between 0ms and 3.75ms, or between 0ms and 37.5ms.

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PAGE FF REGISTER MAP

PAGE (00h)

Format: Unsigned binary

The PAGE command on Page FF provides the ability to configure, control, and monitor all outputs through only one physical address. All subsequent commands that allow for multi-page actions are applied to the corresponding regulators selected by the PAGE (00h) command.

Bits	Access	Bit Name	Description
7:0	R/W	PAGE	8'b00000000: V_{OUT1} (Page 0) 8'b00000001: V_{OUT2} (Page 1) 8'b00000002: V_{OUT3} (Page 2) 8'b00000003: LDO (Page 3) 8'b11111111: All rails (Page FF) Others: Ineffective input

OPERATION (01h)

Format: Unsigned binary

The OPERATION command on Page FF configures the on/off state of the converter's output.

Bits	Access	Bit Name	Description
7	R/W	OPERATION	1'b1: The output is on 1'b0: The output is off
6:0	R/W	RESERVED	Reserved.

CLEAR_FAULTS (03h)

The CLEAR_FAULTS command on Page FF clears any fault bits in the following status registers: STATUS_BYTE (78h), STATUS_WORD (79h), STATUS_VOUT (7Ah), STATUS_IOUT (7Bh), STATUS_INPUT (7Ch), STATUS_TEMPERATURE (7Dh), STATUS_CML (7Eh), and STATUS_MFR_SPECIFIC (80h).

This command is write-only. There is no data byte for this command.

WRITE_PROTECT (10h)

Format: Unsigned binary

The WRITE_PROTECT command on Page FF controls writing to the converter. The intent of this command is to provide protection against accidental changes. It is not intended to provide protection against deliberate changes to the converter's configuration or operation. All the supported commands may have their parameters read, regardless of the WRITE_PROTECT settings.

Bits	Access	Bit Name	Description
7:0	R/W	WRITE_PROTECT	8'b10000000: Disable all writes except to the WRITE_PROTECT command 8'b 01000000: Disable all writes except to the WRITE_PROTECT, OPERATION, and PAGE commands 8'b 00100000: Disable all writes except to the WRITE_PROTECT, OPERATION, PAGE, and VOUT_COMMAND commands 8'b 00000000: Enable writes to all commands Others: Ineffective input

STORE_USER_ALL (15h)

The STORE_USER_ALL command on Page FF instructs the MPQ7928 to copy the contents of the operating memory to the matching locations in the OTP, excluding the internal trim registers. This process occurs when MPQ7928 receives a STORE_USER_ALL command from the digital interface.

This command is write-only. There is no data byte for this command.

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RESTORE_USER_ALL (16h)

The RESTORE_USER_ALL command on Page FF instructs the MPQ7928 to copy the contents from the OTP and overwrite the matching locations in the operating memory, excluding the trim registers. Any items in the OTP that do not have matching locations in the operating memory are ignored.

The RESTORE_USER_ALL command can be used with the MPQ7928 is operating. However, the MPQ7928 may be unresponsive during the operation with unpredictable or undesirable results.

This command is write-only. There is no data byte for this command.

VOUT_COMMAND (21h)

Format: Unsigned binary

The VOUT_COMMAND command on Page FF sets the MPQ7928's output voltages.

Bits	Access	Bit Name	Description
15:6	R/W	RESERVED	Reserved.
5:0	R/W	VOUT_CMD	V_{OUT1} = Bits[3:0] x 100mV + 2.5V, 2.5V to 4V. 100mV/step V_{OUT2} = Bits[5:0] x 50mV + 0.6V, 0.6V to 3.75V. 50mV/step V_{OUT3} = Bits[5:0] x 50mV + 0.6V, 0.6V to 2.55V (is clamped to 2.55V when V_{OUT3} is set to exceed 2.55V). 50mV/step V_{LDO} = Bits[5:0] x 50mV + 0.6V, 0.6V to 3.75V. 50mV/step

TON_RISE (61h)

Format: Unsigned binary

The TON_RISE command on Page FF sets the soft-start time for all bucks. Writing to this register is not valid for Page 3 (the LDO rail).

Bits	Access	Bit Name	Description
15:3	R/W	RESERVED	Reserved.
2:0	R/W	TON_RISE	The soft-start times can be calculated with the following equation: Soft-Start Time = (TON_RISE + 2) x 0.25ms The time ranges between 0.5ms and 2.25ms.

FREQUENCY_DITHER (C4h)

Format: Unsigned binary

The FREQUENCY_DITHER command on Page FF configures the frequency spread spectrum (FSS) parameters.

Bits	Access	Bit Name	Description
7	R/W	FSS_EN	Enables FSS control. 1'b0: Disabled 1'b1: Enabled
6:5	R/W	RESERVED	Reserved.
4	R/W	SSM_RAN	1'b0: ±5% spread spectrum modulation range 1'b1: ±10% spread spectrum modulation range
3:1	R/W	RESERVED	Reserved.
0	R/W	SSM_FRE	1'b0: 4.5kHz spread spectrum modulation frequency 1'b1: 9kHz spread spectrum modulation frequency

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PG_MAPPING (C5h)

Format: Unsigned binary

The PG_MAPPING command on Page FF configures PG mapping for certain faults.

Bits	Access	Bit Name	Description
7:4	R/W	RESERVED	Reserved.
3	R/W	PM_CML_PG#_ MAPPING	Sets the PG mapping for PMBus communication failures. 1'b0: A PMBus communication failure causes PG to go low and register assertion 1'b1: A PMBus communication failure causes register assertion only
2	R/W	PM_CRC_PG#_ MAPPING	Sets the PG mapping for PMBus CRC faults. 1'b0: A PMBus CRC failure causes PG to go low and register assertion 1'b1: A PMBus CRC failure causes register assertion only
1:0	R/W	RESERVED	Reserved.

PROTECTION_CONFIG (CBh)

Format: Unsigned binary

The PROTECTION_CONFIG command on Page FF enables packet error checking (PEC).

Bits	Access	Bit Name	Description
7:1	R/W	RESERVED	Reserved.
0	R/W	PEC_REQ	Indicates whether PEC is required. 1'b0: PEC is disabled 1'b1: PEC is optional

PG_CONFIG (CCh)

Format: Unsigned binary

The PG_CONFIG command on Page FF configures the PG parameters.

Bits	Access	Bit Name	Description
7:4	R/W	RESERVED	Reserved.
3	R/W	PG_OUT	Sets the PG V_{OUT}. 1'b0: 1.8V 1'b1: 3.3V
2:1	R/W	PG_DELAY	Sets the PG de-assertion delay. 2'b00: Immediate 2'b01: 2ms 2'b10: 5ms 2'b11: 10ms
0	R/W	PG_THRESHOLD	Sets the PG threshold. 1'b0: ±4% 1'b1: ±6%

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GATE_DRIVE STRENGTH (CDh)

Format: Unsigned binary

The GATE_DRIVE STRENGTH command on Page FF configures the drive strength for buck 3's low-/high-side gate.

Bits	Access	Bit Name	Description
7:2	R/W	RESERVED	Reserved.
1:0	R/W	GATE_STR	2'b00: Low gate drive strength 2'b01: Medium-low gate drive strength 2'b10: Medium-high gate drive strength 2'b11: High gate drive strength

LIGHT_LOAD (CEh)

Format: Unsigned binary

The LIGHT_LOAD command on Page FF configures the light-load operation mode and enables the output discharge function.

Bits	Access	Bit Name	Description
7:2	R/W	RESERVED	Reserved.
1	R/W	OUT_DIS	1'b0: Output discharge disabled 1'b1: Output discharge enabled
0	R/W	LIGHT_MODE	1'b0: Continuous conduction mode (CCM) 1'b1: Discontinuous conduction mode (DCM)

TON_OFF_DELAY (CFh)

Format: Unsigned binary

The TON_OFF_DELAY command on Page FF configures the turn-off and turn-on times.

Bits	Access	Bit Name	Description
7:4	R/W	ON_DELAY	Sets the turn-on delay, calculated with the following equation: Turn-On Delay = ON_DELAY x DELAY_SCALE Where DELAY_SCALE can range between 0ms and 3.75ms, or between 0ms and 37.5ms.
3:0	R/W	OFF_DELAY	Sets the turn-off delay, calculated with the following equation: Turn-Off Delay = OFF_DELAY x DELAY_SCALE Where DELAY_SCALE can range between 0ms and 3.75ms, or between 0ms and 37.5ms.

TON_OFF_SCALE (D0h)

Format: Unsigned binary

The TON_OFF_SCALE command on Page FF configures the scale for the turn-off and turn-on times.

Bits	Access	Bit Name	Description
7:1	R/W	RESERVED	Reserved.
0	R/W	DELAY_SCALE	Sets the delay scale. 1'b0: Scale = 0.25ms. The delay ranges between 0ms and 3.75ms 1'b1: Scale = 2.5ms. The delay ranges between 0ms and 37.5ms

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FREQUENCY_ILIM_SCALE (D1h)

Format: Unsigned binary

The FREQUENCY_ILIM_SCALE command on Page FF configures the switching frequency (f_{SW}) and current limit (I_{LIMIT}) for buck 1, buck 2, and buck 3.

Bits	Access	Bit Name	Description
7:2	R/W	RESERVED	Reserved.
1	R/W	FREQUENCY	Sets f_{SW} for buck 1, buck 2, and buck 3. 1'b0: 2.2MHz 1'b1: 3.3MHz
0	R/W	ILIM	Sets I_{LIMIT} for buck 1, buck 2, and buck 3. 1'b0: 100% of the current limit 1'b1: 125% of the current limit

VIN_START_STOP (D2h)

Format: Unsigned binary

The VIN_START_STOP command on Page FF configures the start voltage for VIN (V_{IN_START}) and stop voltage for VIN (V_{IN_STOP}). To modify this register, V_{IN_START} and V_{IN_STOP} must both be set to the under-voltage lockout (UVLO) threshold, or they must both be set to other values.

Bits	Access	Bit Name	Description
7:4	R/W	RESERVED	Reserved.
3:2	R/W	VIN_START	Sets V_{IN_START}. 2'b00: UVLO threshold 2'b01: 4V 2'b10: 5V 2'b11: 6V
1:0	R/W	VIN_STOP	Sets V_{IN_STOP}. 2'b00: UVLO threshold 2'b01: 3.5V 2'b10: 4.5V 2'b11: 5.5V

ADDRESS (D3h)

Format: Unsigned binary

The ADDRESS command on Page FF sets the digital interface communication address.

Bits	Access	Bit Name	Description
7:4	R/W	RESERVED	Reserved.
3:0	R/W	ADDRESS	Sets the 4 bits of the digital address.

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APPLICATION INFORMATION

Figure 14 shows the MPQ7928's typical application circuit.

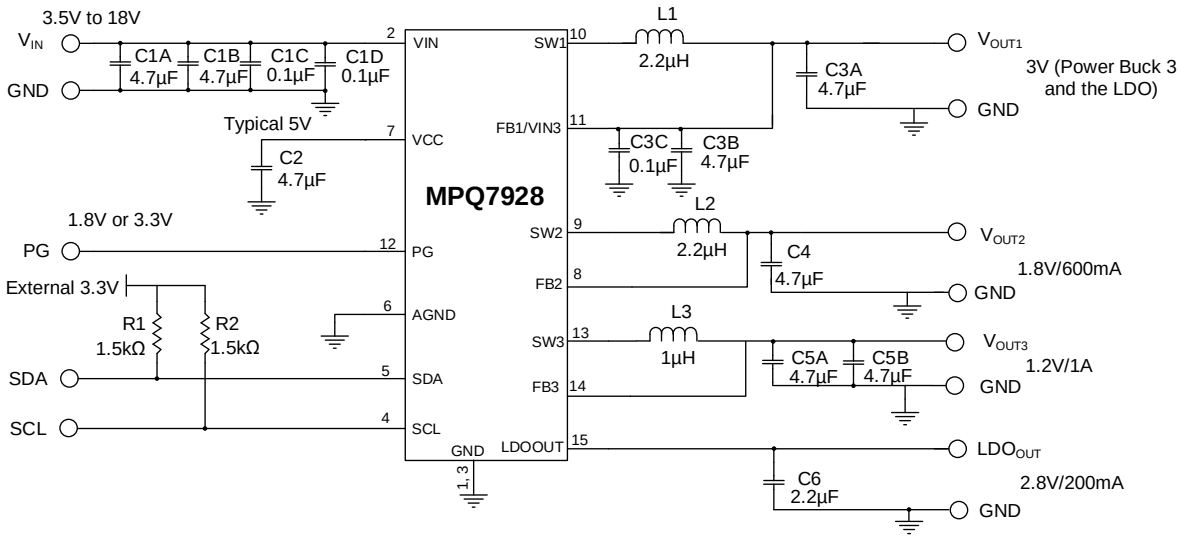

Figure 14: Typical Application Circuit (V_{OUT1} = 3V, V_{OUT2} = 1.8V, V_{OUT3} = 1.2V, V_{LDO} = 2.5V)

Table 3: Design Guide Index

Pin #	Pin Name	Component	Design Guide Index
14	FB3	-	Setting the Output Voltage (FB1, Pin 11; FB2, Pin 8; FB3, Pin 14)
8	FB2	-	Setting the Output Voltage (FB1, Pin 11; FB2, Pin 8; FB3, Pin 14)
11	FB1/VIN3	C3B, C3C	Setting the Output Voltage (FB1, Pin 11; FB2, Pin 8; FB3, Pin 14) Selecting the Input Capacitors (VIN, Pin 2; VIN3, Pin 11)
2	VIN	C1A, C1B, C1C, C1D	Selecting the Input Capacitors (VIN, Pin 2; VIN3, Pin 11)
9	SW2	L2, C4	Selecting the Output Capacitors (SW2, Pin 9; SW1, Pin 10; SW3, Pin 13; LDOOUT, Pin 15) Selecting the Inductors (SW2, Pin 9; SW1, Pin 10; SW3, Pin 13)
10	SW1	L1, C3A	Selecting the Output Capacitors (SW2, Pin 9; SW1, Pin 10; SW3, Pin 13; LDOOUT, Pin 15) Selecting the Inductors (SW2, Pin 9; SW1, Pin 10; SW3, Pin 13)
13	SW3	L3, C5A, C5B	Selecting the Output Capacitors (SW2, Pin 9; SW1, Pin 10; SW3, Pin 13; LDOOUT, Pin 15) Selecting the Inductors (SW2, Pin 9; SW1, Pin 10; SW3, Pin 13)
15	LDOOUT	C6	Selecting the Output Capacitors (SW2, Pin 9; SW1, Pin 10; SW3, Pin 13; LDOOUT, Pin 15)
7	VCC	C2	Internal VCC (VCC, Pin 7)
4	SCL	-	I^2C Interface (SCL, Pin 4; SDA, Pin 5)
5	SDA	-	I^2C Interface (SCL, Pin 4; SDA, Pin 5)
12	PG	-	Power Good Indicator (PG, Pin 12)
1, 3	GND	-	GND Connection (GND, Pins 1 and 3; AGND, Pin 6)
6	AGND	-	GND Connection (GND, Pins 1 and 3; AGND, Pin 6)

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Setting the Output Voltage (FB1, Pin 11; FB2, Pin 8; FB3, Pin 14)

The OTP command VOUT_COMMAND (21h on Page 0, Page 1, Page 2, Page 3, and Page FF) sets the output voltages. Write to the VOUT_CMD bits on Page FF to set each rail's output voltage. The output voltage (V_{OUT1}, V_{OUT2}, V_{OUT3}, and V_{LDO}) can be calculated with Equation (1), Equation (2), Equation (3), and Equation (4), respectively:

$$V_{OUT1}(V)= VOUT_CMD,Bits[3:0]\times 0.1+2.5 \quad (1)$$

$$V_{OUT2}(V)= VOUT_CMD,Bits[5:0]\times 0.05+0.6 \quad (2)$$

$$V_{OUT3}(V)= VOUT_CMD,Bits[5:0]\times 0.05+0.6 \quad (3)$$

$$V_{LDO}(V)= VOUT_CMD,Bits[5:0]\times 0.05+0.6 \quad (4)$$

Selecting the Input Capacitors (VIN, Pin 2; VIN3, Pin 11)

The step-down converter has a discontinuous input current, and requires a capacitor to supply AC current to the converter while maintaining the DC input voltage. For the best performance, use low-ESR capacitors. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients.

It is strongly recommended to use another lower-value capacitor (e.g. 0.1µF) with a small package size (0603) to absorb high-frequency switching noise. Place this capacitor as close to VIN and GND as possible.

Since the input capacitor (C_{IN}) absorbs the input switching current, it requires an adequate ripple current rating. The RMS current in the input capacitor can be estimated with Equation (5):

$$I_{CIN}=I_{LOAD}\times\sqrt{\frac{V_{OUT}}{V_{IN}}\times(1-\frac{V_{OUT}}{V_{IN}})} \quad (5)$$

The worst-case condition occurs at V_{IN} = 2 x V_{OUT}, calculated with Equation (6):

$$I_{CIN}=\frac{I_{LOAD}}{2} \quad (6)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitor can be electrolytic, tantalum, or ceramic. When using electrolytic or tantalum capacitors, add a small, high-quality ceramic capacitor (e.g. 0.1µF) as close to the IC as possible. When using ceramic capacitors, ensure that they have enough capacitance to provide a sufficient charge to prevent excessive input voltage ripple. The input voltage ripple caused by the capacitance can be estimated with Equation (7):

$$\Delta V_{IN}=\frac{I_{LOAD}}{f_{SW}\times C_{IN}}\times\frac{V_{OUT}}{V_{IN}}\times(1-\frac{V_{OUT}}{V_{IN}}) \quad (7)$$

Selecting the Output Capacitors (SW2, Pin 9; SW1, Pin 10; SW3, Pin 13; LDOOUT, Pin 15)

The output capacitor maintains the DC output voltage. Use ceramic, tantalum, or low-ESR electrolytic capacitors. For the best results, use low-ESR capacitors to keep the output voltage ripple low. The buck regulator's output voltage ripple can be estimated with Equation (8):

$$\Delta V_{OUT}=\frac{V_{OUT}}{f_{SW}\times L}\times(1-\frac{V_{OUT}}{V_{IN}})\times(R_{ESR}+\frac{1}{8\times f_{SW}\times C_{OUT}}) \quad (8)$$

Where L is the inductor value, and R_{ESR} is the output capacitor's equivalent series resistance (ESR).

For ceramic capacitors, the capacitance dominates the impedance at the switching frequency and causes the majority of the output voltage ripple.

For simplification, the output voltage ripple can be estimated with Equation (9):

$$\Delta V_{OUT}=\frac{V_{OUT}}{8\times f_{SW}^{2}\times L\times C_{OUT}}\times(1-\frac{V_{OUT}}{V_{IN}}) \quad (9)$$

For tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be calculated with Equation (10):

$$\Delta V_{OUT}=\frac{V_{OUT}}{f_{SW}\times L}\times(1-\frac{V_{OUT}}{V_{IN}})\times R_{ESR} \quad (10)$$

The characteristics of the output capacitor also affect the stability of the regulation system. The MPQ7928 can be optimized for a wide range of capacitance and ESR values.

The LDO is specifically designed to work with a standard ceramic output capacitor to save

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space and improve performance. The LDO charges the output capacitor during the start-up stage, and the charge current is equal to the LDO current limit subtracted by the LDO load current. There is an internal under-voltage blanking time with a minimum 385µs, and the output capacitor must be fully charged during this period.

For example, if there is a constant 200mA load during start-up and the LDO voltage is set to 2.8V, the output capacitor should be below 6.9µF to be fully charged. A 2.2µF ceramic capacitor (e.g. GRM21BR71C225KA12L, 16V, X7R) is recommended for most applications.

A higher output capacitance is possible if the load current during the start-up stage is kept sufficiently low. The maximum effective output capacitance can be estimated with Equation (11):

$$C_{MAX} = (I_{LIM_MIN} - I_{LOAD}) \times BT / V_{LDO} \quad (11)$$

Where I_{LIM_MIN} = 280mA, and BT = 385µs.

For example, if the load current is a constant 10mA during start-up and the set LDO voltage is 2.8V, the maximum allowed effective capacitance is (0.27A / 2.8V x 385µs), which is about 37µF.

Selecting the Inductors (SW2, Pin 9; SW1, Pin 10; SW3, Pin 13)

For most applications, it is recommended to use a 1µH to 10µH inductor with a DC current rating at least 25% higher than the maximum load current. For higher efficiency, choose an inductor with a lower DC resistance. A larger-value inductor results in less ripple current and a lower output ripple voltage, but also has a larger physical size, higher series resistance, and lower saturation current.

A good rule to determine the inductance is to allow the inductor ripple current to be approximately 30% of the maximum load current. The inductance can be calculated with Equation (12):

$$L = \frac{V_{OUT}}{f_{SW} \times \Delta I_L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (12)$$

Where ΔI_L is the peak-to-peak inductor ripple current.

Choose the inductor ripple current to be approximately 30% of the maximum load current. The maximum inductor peak current can be calculated with Equation (13):

$$I_{LP} = I_{LOAD} + \frac{V_{OUT}}{2 \times f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (13)$$

Internal VCC (VCC, Pin 7)

The VCC capacitor (C2) should be between 1µF and 10µF. Generally, a 2.2µF or 4.7µF ceramic capacitor is recommended.

Most of the internal circuitry is powered by the internal 5V VCC regulator. This regulator uses VIN as its input and operates across the full V_{IN} range. When V_{IN} exceeds 5V, V_{CC} is in full regulation. When V_{IN} drops below 5V, the V_{CC} output degrades.

I²C Interface (SCL, Pin 4; SDA, Pin 5)

The MPQ7928 works as a slave-only device, which supports up to 1Mbps of bidirectional data transfer in fast mode, adding flexibility to the power supply solution. See the I²C Interface section on page 37 for details.

The SCL and SDA lines are externally pulled to an external voltage (e.g. 3.3V) with a resistor (e.g. 1kΩ).

Power Good Indicator (PG, Pin 12)

The PG pin integrates an internal, push-pull structure, so no external components are required.

GND Connection (GND, Pins 1 and 3; AGND, Pin 6)

See the PCB Layout Guidelines section on page 66 for more details.

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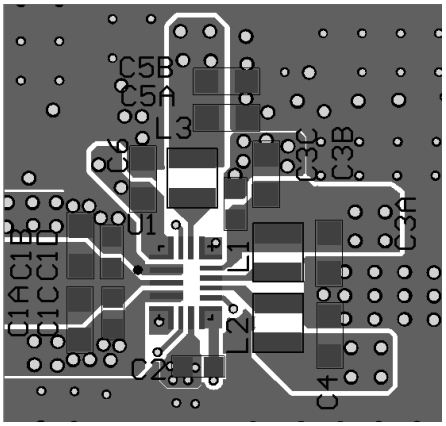
PCB Layout Guidelines (13)

Efficient PCB layout, especially for input capacitor placement, is critical for stable operation. A 4-layer layout is strongly recommended to improve thermal performance. For the best results, refer to Figure 15 and follow the guidelines below:

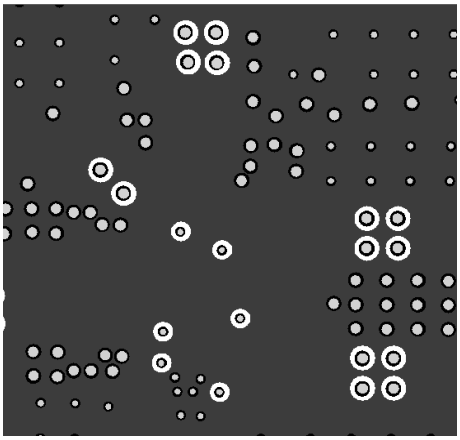
1. Place the symmetric input capacitors as close to VIN and GND as possible.
2. Use a large ground plane to connect to GND directly.
3. Ensure that the high-current paths at GND and VIN have short, direct, and wide traces.
4. Place the ceramic input capacitor, especially the small package size (0603) input bypass capacitor, as close to VIN, VIN3, and GND as possible to minimize high-frequency noise.
5. Keep the connection between the input capacitor and VIN as short and wide as possible.
6. Place the VCC capacitor as close to VCC and AGND as possible.
7. Route SW away from sensitive analog areas, such as FB.
8. Ensure that the trace between FB and the output is as short as possible.
9. Use multiple vias to connect the power planes to the internal layers.

Note:

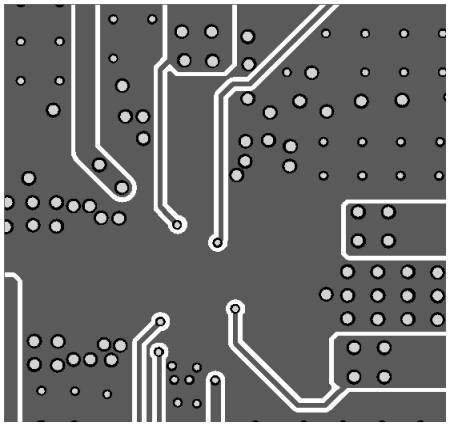
13) The recommended PCB layout is based on Figure 16 on page 67.



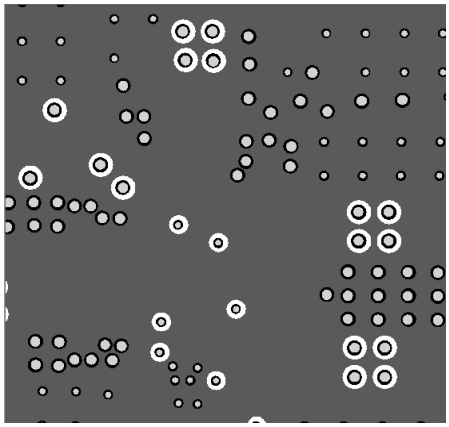
Top Layer



Inner Layer 1



Inner Layer 2



Bottom Layer

Figure 15: Recommended PCB Layout

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TYPICAL APPLICATION CIRCUITS

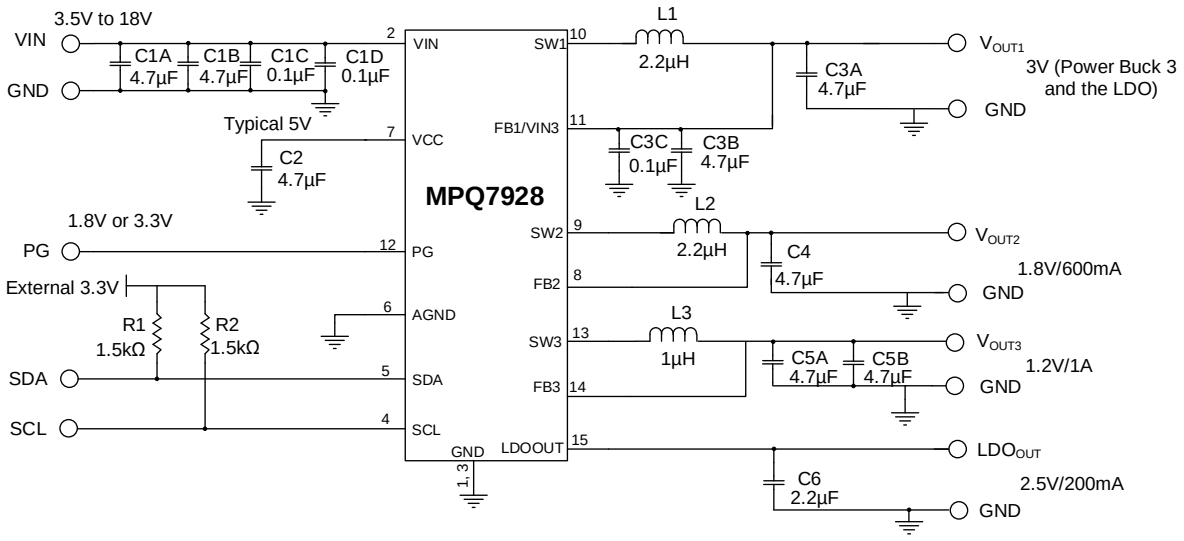

Figure 16: Typical Application Circuit (V_{OUT1} = 3V, V_{OUT2} = 1.8V, V_{OUT3} = 1.2V, V_{LDO} = 2.5V)

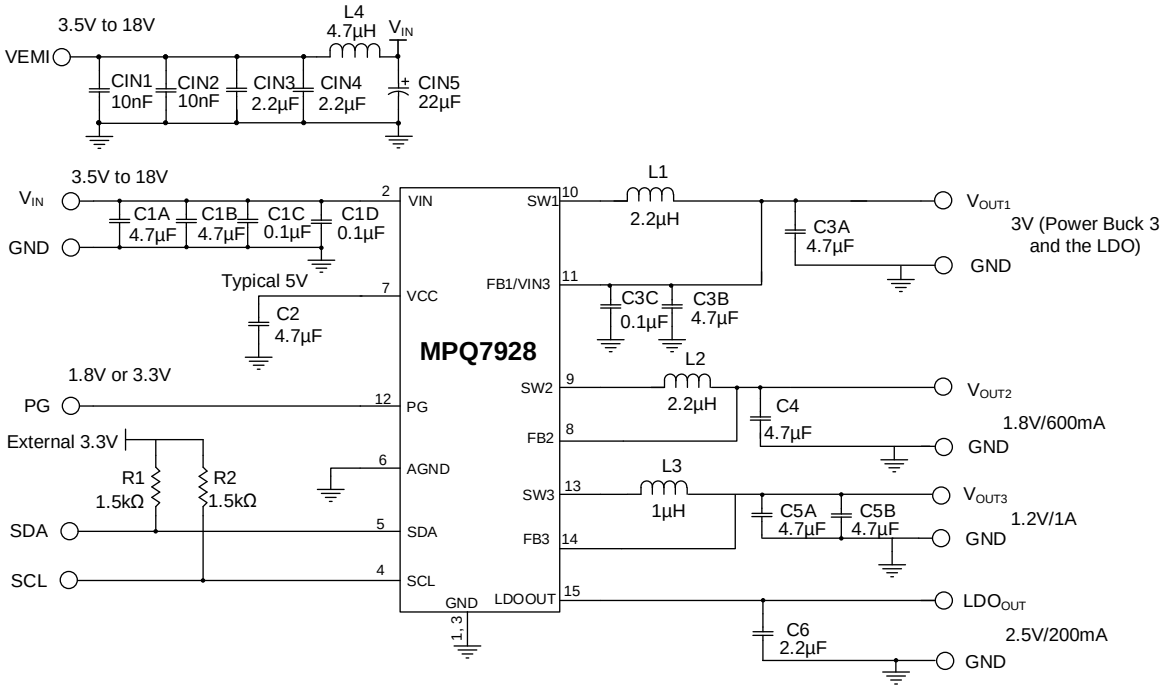

Figure 17: Typical Application Circuit (V_{OUT1} = 3V, V_{OUT2} = 1.8V, V_{OUT3} = 1.2V, V_{LDO} = 2.5V with EMI Filters)

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TYPICAL APPLICATION CIRCUITS *(continued)*

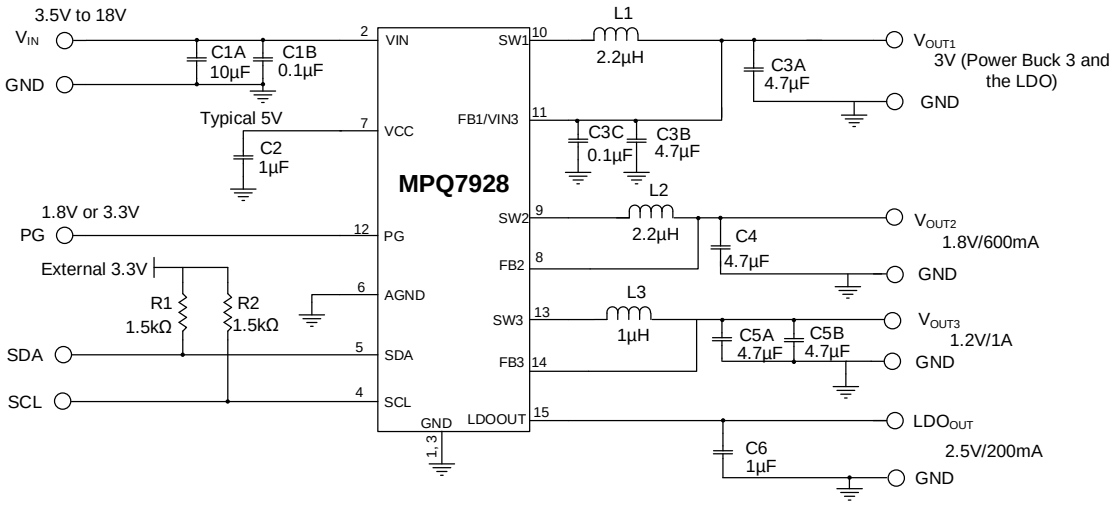

Figure 18: Typical Application Circuit (V_{OUT1} = 3V, V_{OUT2} = 1.8V, V_{OUT3} = 1.2V, V_{LDO} = 2.5V with Minimal External Components)

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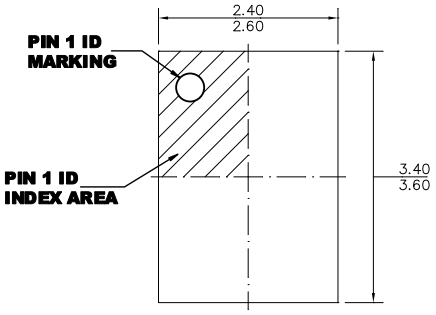
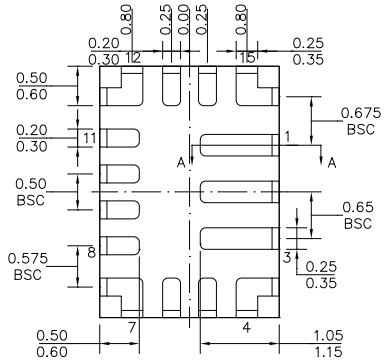
PACKAGE INFORMATION

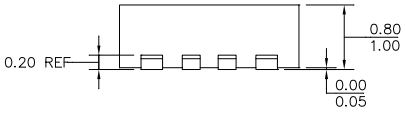
QFN-15 (2.5mmx3.5mm)
Wettable Flank



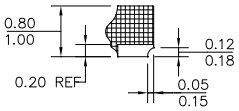
TOP VIEW



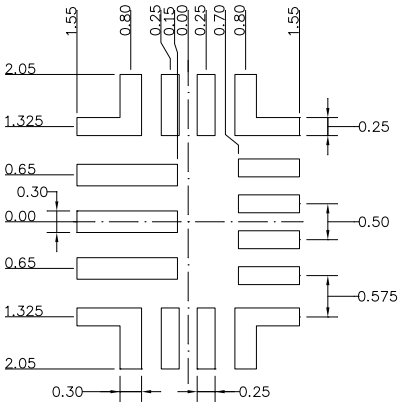
BOTTOM VIEW



SIDE VIEW



SECTION A-A



RECOMMENDED LAND PATTERN

NOTE:

1) THE LEAD SIDE IS WETTABLE.
2) ALL DIMENSIONS ARE IN MILLIMETERS.
3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

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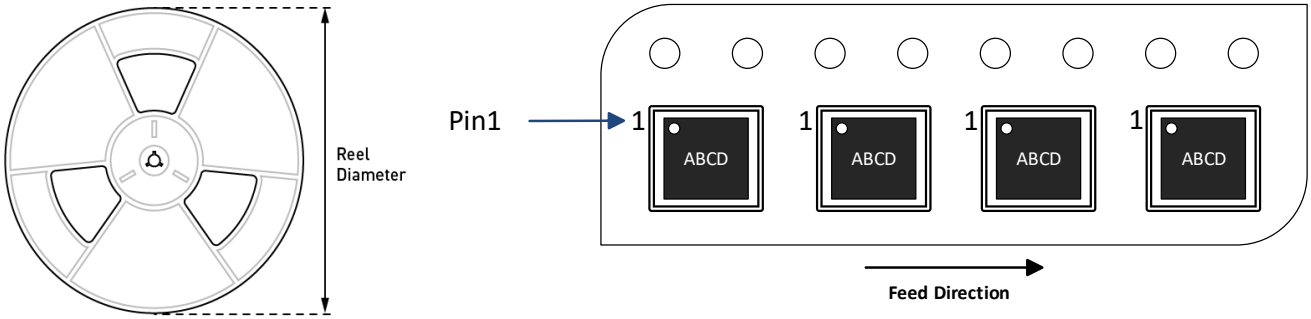
CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube (14)	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPQ7928GRHE-xxxx-AEC1-Z	QFN-15 (2.5mmx3.5mm)	5000	N/A	N/A	13in	12mm	8mm

Note:

14) N/A indicates “not available” in tubes. For 500-pieces tape & reel prototype quantities, contact the factory. (The order code for the 500-piece partial reel is “-P”; the tape & reel dimensions are the same as the full reel.)

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REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	12/6/2023	Initial Release	-

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