MPX2001

All-in-One Flyback Controller with Integrated Primary and Secondary Synchronous Rectification Driver with Capacitive Isolation

DESCRIPTION

The MPX2001 is an all-in-one flyback controller solution. The MPX2001 integrates a primary driving circuit, secondary controller, and synchronous rectification driver all in one chip, maintaining the benefits of both primary-side regulation (PSR) and secondary-side regulation (SSR).

With the MPX2001, system complexity can be reduced since no feedback circuit is needed. Therefore, the total BOM cost is reduced. At the same time, a synchronous rectifier (SR) can be matched perfectly with the driving signal of the primary-side MOSFET. With this feature, the SR can operate safely in continuous conduction mode (CCM), which helps increase overall efficiency and provides the design with more flexibility.

The MPX2001 features advanced protections, including primary-sense output over-voltage protection (OVP), primary over-current protection (POCP), real secondary-sense output overload protection (OLP), internal/external brown-in/brown-out (B/O, B/I), short-circuit protection (SCP), current-sensing short protection (SSP), internal thermal shutdown, under-voltage lockout (UVLO), and an externally triggered protection (Ext.P).

The MPX2001 is available in SOICW20 and SOICW20-19 packages.

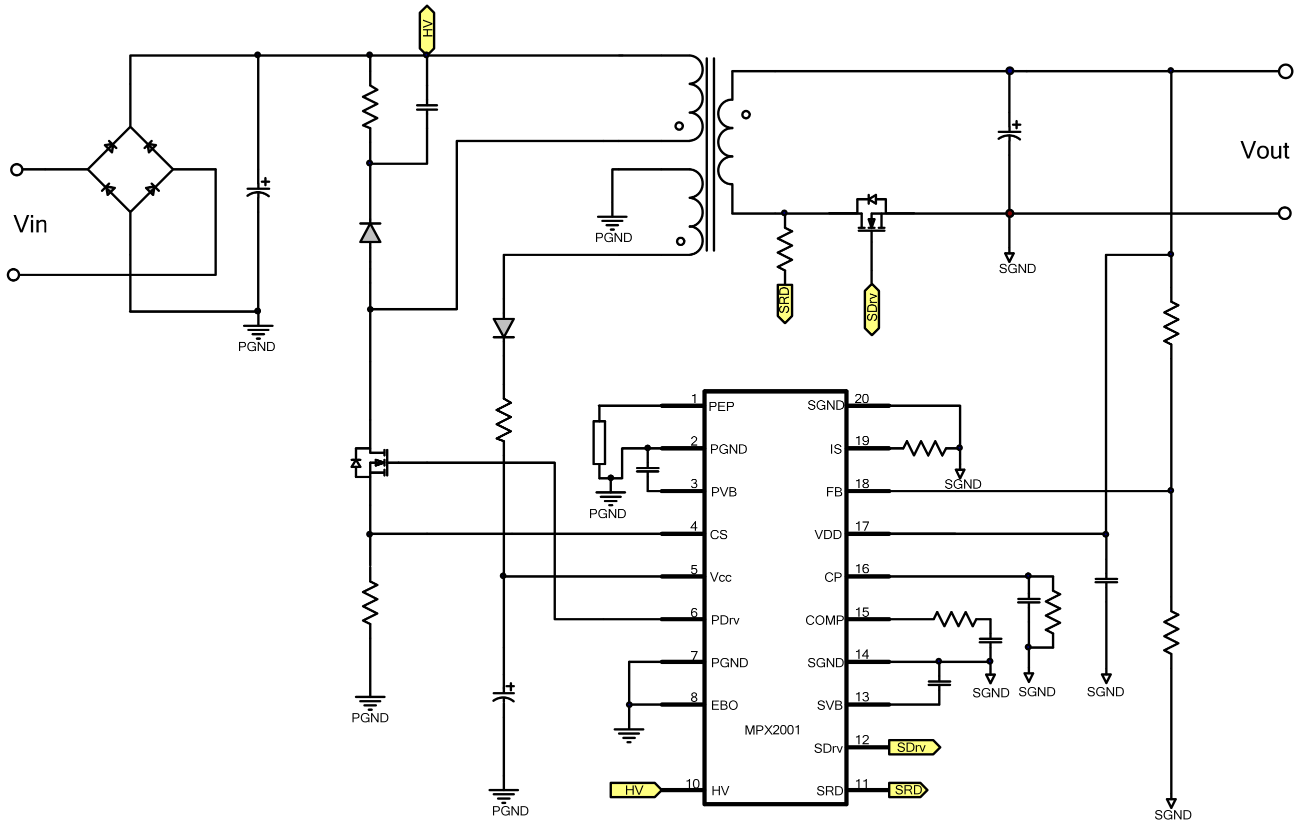
FEATURES

- Isolation Voltage >4500Vrms
- UL1577 and IEC 62368 Safety Approved
- 100% Production HIPOT Test at 4500Vrms/50Hz
- 650V Integrated HV Current Source
- 200V Integrated SR Controller, Supporting both DCM and CCM Operation
- Incorporates Primary Driving Circuit, Secondary Controller, and Synchronous Rectification Driver
- Extremely Low Operating Current in Standby Mode
- Frequency Modulation and Peak Current Mode Control with Slope Compensation, Line Compensation, and Leading Edge Blanking
- Adjustable Cable Drop Compensation
- OVP, POCP, Real Secondary-Sense Output OLP, Internal/External B/O and B/I, SCP, Current-Sensing Short Protection, Internal Thermal Shutdown, UVLO, and Ext.P
- Available in a SOICW20 and SOICW20-19 Packages

APPLICATIONS

- AC/DC Adapters
- Power Supply for Appliances
- Offline Battery Chargers
- High Efficiency, High-Current Power Supplies, Etc.

TYPICAL APPLICATION



ORDERING INFORMATION

Part Number	Package	Top Marking
MPX2001GY*	SOICW20	*See Below*
MPX2001GYE**	SOICW20-19	*See Below*

* For Tape & Reel, add suffix –Z (e.g. MPX2001GY–Z)
** For Tape & Reel, add suffix –Z (e.g. MPX2001GYE–Z)

TOP MARKING

MPSYYWW
MPX2001
LLLLLLLLL

MPS: MPS prefix
YY: Year code
WW: Week code
MPX2001: Product code of MPX2001GY/MPX2001GYE
LLLLLLLLL: Lot number

EVALUATION KIT EVKT-MPX2001-45-PD

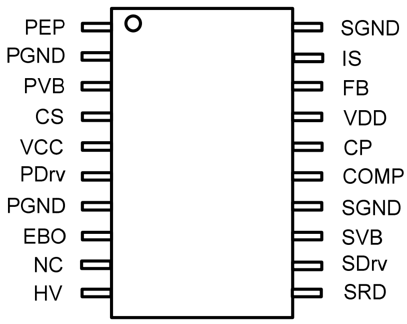
EVKT-MPX2001-45-PD Kit contents: (Items below can be ordered separately).

#	Part Number	Item	Quantity
1	EVX2001-Y-02A	MPX2001 45W USB PD evaluation board	1
2	Tdrive-MPX2001	USB flash drive that stores the user guide, USBCEE test board files	1
3		USB C to USB C cable	1
4		USB A to mini USB cable	1
5		USBCEE test board	1

Order direct from www.MonolithicPower.com or our distributors.

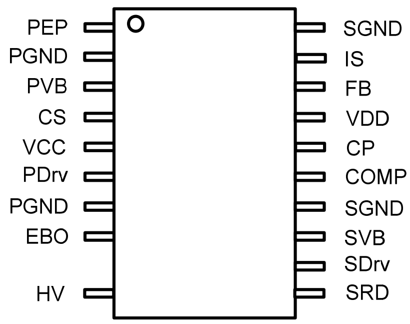
PACKAGE REFERENCE

TOP VIEW
MPX2001GY



SOICW20

TOP VIEW
MPX2001GYE



SOICW20-19

ABSOLUTE MAXIMUM RATINGS (1)

HV to PGND.................................-0.3V to 650V
SRD to SGND ....-1V to 200V
VCC to PGND ....-0.3V to 35V
PDrv to PGND................................-0.3V to 16V
SDrv to SGND................................-0.3V to 16V
VDD to SGND ....-0.3V to 35V
PVB, CS, PEP, EBO to PGND ......-0.3V to 6.5V
SVB, COMP, CP, FB, IS to SGND ....
....-0.3V to 6.5V
Continuous power dissipation (T_A = +25°C) (2)
SOICW20 ....2.3W
SOICW20-19...2.3W
Junction temperature .... 150°C
Thermal shutdown .... 150°C
Thermal shutdown hysteresis..................... 40°C
Lead temperature..................................... 260°C
Storage temperature.................-60°C to +150°C
ESD capability human body model (except VCC, VDD, SRD and HV)...................................4.0kV
ESD capability human body model (VCC, VDD) 3.5kV
ESD capability human body model (SRD) 2.0kV
ESD capability human body model (HV)....800V

Recommended Operating Conditions (3)

Operating junction temp (T_J).....-40°C to +125°C
VCC to PGND .... 9V to 24V
VDD to SGND .... 4.75V to 32V

Thermal Resistance (4)	θ_{JA}	θ_{JC}	
SOICW20	55	30	°C/W
SOICW20-19	55	30	°C/W

NOTES:
1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

Typical value tested at T_J = -40°C to 125°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Insulation						
Isolation voltage	V_{ISO}	50/60Hz	4.5			kVrms
Primary Side (HV)						
Break-down voltage	V_{HV-BD}	T_J = 25°C	650			V
Leakage current from HV	I_{HV-LK}	V_{DS} = 500V_{DC}			18	µA
Supply current from HV	I_{HV-SP1}	VCC = 12V, V_{HV} = 80~400V, T_J < 110°C	3.9	4.7	5.5	mA
	I_{HV-SP2} (5)	VCC = 12V, V_{HV} = 80~400V, T_J ≥ 110°C		2.3		mA
Brown-in threshold voltage	V_{HV-ON}		95	106	118	V
Brown-out threshold voltage	V_{HV-OFF}		85	96	108	V
Brown-in/out hysteresis	$V_{HV-\Delta}$		7.5	10	12.5	V
Delay time for brown-out	t_{BO}		54	67	80	ms
Primary Side (VCC)						
I_{HV-SP} turn-off voltage	$V_{CC-IOFF}$		13	14.5	16	V
Minimum operation voltage	V_{CC-MIN}		7	8	9	V
$V_{CC-IOFF}$ - V_{CC-MIN}	V_{CC-STW}		5.5	6.5		V
Auto-recovery protection level	V_{CC-AUT}		4.7	5.3	5.9	V
VCC over-voltage protection level	V_{CC-OVP}		24	27	30	V
Operating current	I_{OP}	VCC = 15V, f_S = 80kHz, C_L = 1nF			3.5	mA
Operating current during protection	I_{OP-NS}	VCC = 8V			250	µA
Operating current during latch-off	I_{OP-LO}	VCC = 5V			250	µA
Quiescent current	I_Q	VCC = 12V			300	µA
Primary Side (PDrv)						
Driver voltage high level	V_{High}	C_L = 1nF, VCC = 7V	5			V
		C_L = 1nF, VCC = 12V	9.9			V
Driver voltage clamp level	V_{Clamp}	C_L = 1nF, VCC = 24V	11	13.5	16	V
Driver voltage low level	V_{Low}	C_L = 1nF			100	mV
Driver voltage rise time	t_{Rise}	C_L = 1nF		30		ns
Driver voltage fall time	t_{Fall}	C_L = 1nF		20		ns
Maximum switching frequency	f_{S-Max}	T_J = 25˚C	82	85	89	kHz
Sensing short protection (5)	t_{ON-Max}			10		µs
Time to trigger primary OCP	t_{OCP}		56	69	82	ms
Soft-start duration	t_{Soft}		9	11	15	ms
Minimal switching frequency during soft start	f_{S-Soft}			20		kHz

ELECTRICAL CHARACTERISTICS *(continued)*

Typical value tested at T_J = -40°C to 125°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Primary Side (CS)						
Threshold for SCP	V_{SCP}		0.83	0.9	0.97	V
Maximum peak current limitation	$V_{IPK\text{-}Max}$		0.57	0.6	0.63	V
Minimum peak current limitation	$V_{IPK\text{-}Min}$			0.15		V
Jittering amplitude	ΔV_{IPK}	V_{IPK} = 0.6V	±2%	±2.5%	±3%	$V_{IPK\text{-}Max}$
Jittering period (5)				320		cycles
f_{Sync} at which i_{PK} foldback starts	$f_{Sync\text{-}H}$			42		kHz
f_{Sync} at which i_{PK} foldback stops	$f_{Sync\text{-}L}$			20		kHz
Slope of the compensation ramp	S_{RAMP}	f_S = 65kHz	14	20	26	mV/µs
LEB for current limitation	$t_{LEB\text{-}L}$			276		ns
LEB for SCP	$t_{LEB\text{-}S}$			235		ns
ΔI_{HVCS} / ΔV_{HV} ratio	K_{HVCS}			0.51		µA/V
CS sourcing current	I_{HVCS}	V_{HV} = 200V, V_{IPK} = 0.6V, T_J = 25°C		30		µA
		V_{HV} = 375V, V_{IPK} = 0.6V, T_J = 25°C	95	120	150	
Primary Side (PEP)						
Sourcing current from PEP	I_{PEP}	V_{PEP} = 0.5V		100		µA
Saturation voltage	$V_{PEP\text{-}S}$	R_{PEP} = 100kΩ	0.9	1	1.1	V
Protection trigger threshold	$V_{PEP\text{-}T}$		0.45	0.5	0.55	V
Protection trigger delay	$t_{PEP\text{-}T}$			300		µs
Primary Side (EBO)						
Brown-In threshold voltage	$V_{EBO\text{-}ON}$		1.08	1.1	1.12	V
Brown-out threshold voltage	$V_{EBO\text{-}OFF}$		0.98	1	1.02	V
Brown-in/out hysteresis	$V_{EBO\text{-}\Delta}$		0.09	0.1		V
Internal impedance (5)	R_{EBO}	V_{EBO} = 1V	10			MΩ
Primary Side (PVB)						
Regulating voltage	V_{PVB}	I_{PVB} = 0 - 5mA	4.75	5.05	5.35	V
Primary Side – Internal Thermal Protection						
OTP threshold (5)	T_{OTP}			150		°C
Hysteresis to release OTP (5)	T_{Δ}			40		°C
Secondary Side (VDD)						
Operating current	I_{OPS}	VDD = 5V, f_S = 80kHz, C_L = 4.7nF			5	mA
Quiescent current	I_{QS}	VDD = 5V			300	µA
UVLO falling threshold	$V_{DD\text{-}OFF}$		3.6	3.8	4.0	V
UVLO rising threshold	$V_{DD\text{-}ON}$		4.1	4.3	4.5	V
UVLO hysteresis	$V_{DD\text{-}\Delta}$		0.3			V

ELECTRICAL CHARACTERISTICS *(continued)*

Typical value tested at T_J = -40°C to 125°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Secondary Side (FB)						
Feedback reference voltage	V_{REF}		0.991	1	1.009	V
Feedback current	I_{FB}	V_{FB} = 1.25V			50	nA
Secondary Side (SRD, SDrv)						
Regulated forward voltage	V_{SR-F}		-42	-33	-24	mV
Turn-off threshold	V_{SR-OFF}		-10	0	10	mV
Turn-off threshold in t_{ON-min} (5)	$V_{SR-OFF2}$			1.5		V
Turn-on threshold (5)	V_{SR-ON}			0		mV
Turn-off delay (total)	t_{Off-D}	V_D = 0V, C_L = 4.7nF, R_{Drv} = 0Ω, V_{GS} = 2V		80	110	ns
		V_D = 0V, C_L = 10nF, R_{Drv} = 0Ω, V_{GS} = 2V		90	130	ns
Turn-on delay	t_{ON-D}	C_L = 4.7nF		200		ns
Minimal on time	t_{ON-min}		1.3	1.6	1.9	µs
Input current at SRD	I_{SRD}	V_{SRD} = 200V			15	µA
Driver voltage low level	V_{Drv-L}			0.05	0.1	V
Driver voltage clamp level	V_{Clamp}		9	11.5	14	V
Driver voltage high level	V_{Drv-H}	VDD = 10.5V		10.5		V
Driver pull-down resistance	$R_{Pull-down}$	C_L = 4.7nF, VDD = 5V		1	2	Ω
Secondary Side (IS)						
Overload protection threshold	V_{OLP}		38	40	42	mV
Overload protection delay	t_{OLP}	T_J = 25°C	57	68	79	ms
Secondary Side (COMP)						
Transconductance	GM	±10mV/±60mV		2/10k		S
Maximum sink current	I_{sink}		0.5			mA
Maximum source current	I_{source}		0.5			mA
Max threshold for burst mode (5)	V_{Burst}	C_{CP} = 1µF, VDD = 5V		1.7		V
Maximum PFM frequency	f_{s_max}	V_{COMP} = 0V, T_J = 25°C	82	85	89	kHz
Minimal PFM frequency	f_{s_min}	V_{COMP} = 2.5V		20		kHz
Maximum COMP voltage	$V_{COMPmax}$	VDD = 5V	2.5			V
Secondary Side (CP)						
Max supply voltage on CP	$V_{TONS-max}$		2.3	2.4	2.5	V
Min supply voltage on CP	$V_{TONS-min}$			0.52		V
Pull-up resistance	R_{TONS}			200		kΩ
Ratio from CP to V_{REF}	K_{CP}		0.098	0.1	0.102	

ELECTRICAL CHARACTERISTICS *(continued)*

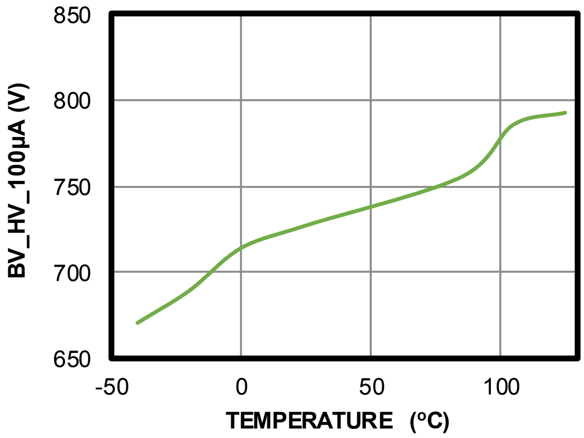
Typical value tested at T_J = -40°C to 125°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Secondary Side (SVB)						
Regulating voltage	V_{SVB}	VDD = 6V	4.75	5	5.25	V
		VDD = 4.7V	4.6			V
UVLO falling threshold	$V_{DD\text{-}OFF}$		3.6	3.8	4.0	V
UVLO rising threshold	$V_{DD\text{-}ON}$		4.1	4.3	4.5	V
UVLO hysteresis	$V_{DD\text{-}\Delta}$		0.3			V
Secondary Side – Internal Thermal Protection						
OTP threshold (5)	T_{OTP}			150		°C
Hysteresis to release OTP (5)	T_{Δ}			40		°C

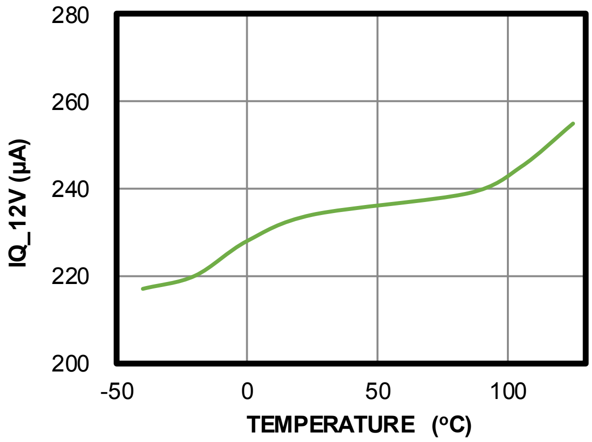
NOTE:
5) These parameters are guaranteed by design.

TYPICAL CHARACTERISTICS

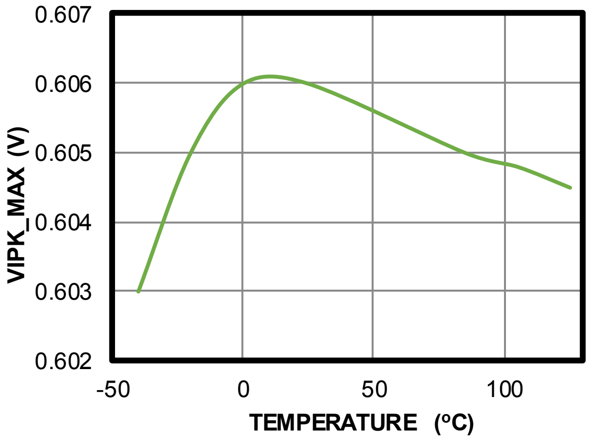
BV_HV_100μA vs. Temperature Chart



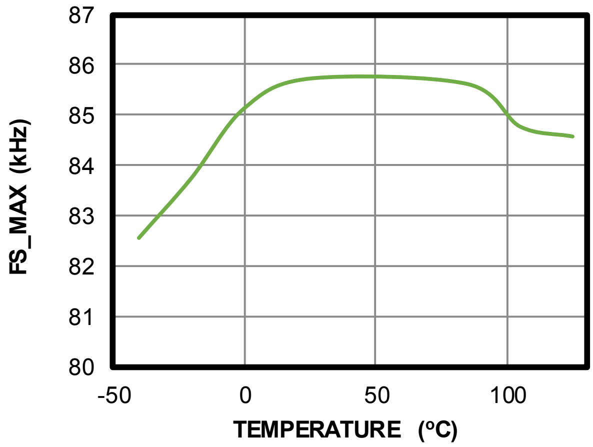
IQ_12V vs. Temperature Chart



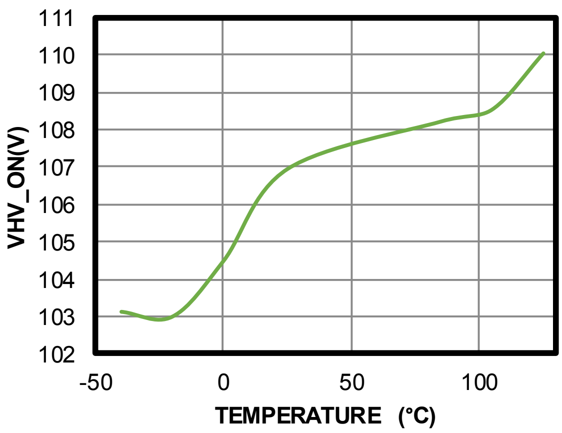
Vipk_max_PT vs. Temperature Chart



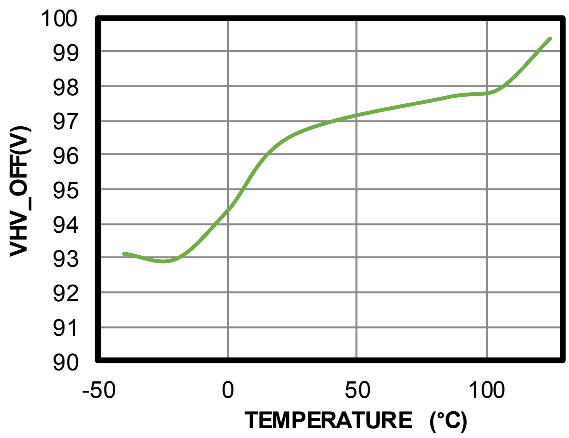
fs_max_PT vs. Temperature Chart



VHV_ON vs. Temperature Chart

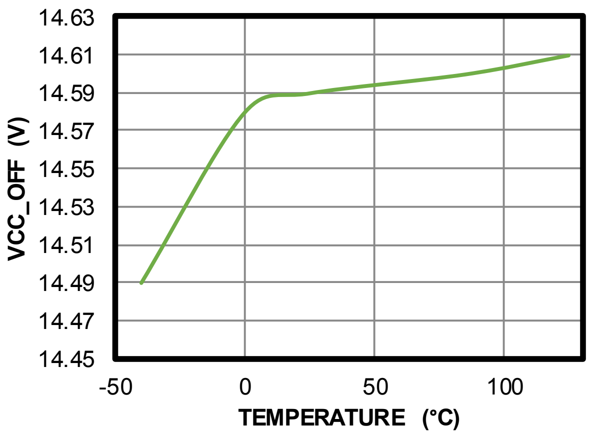


VHV_OFF vs. Temperature Chart

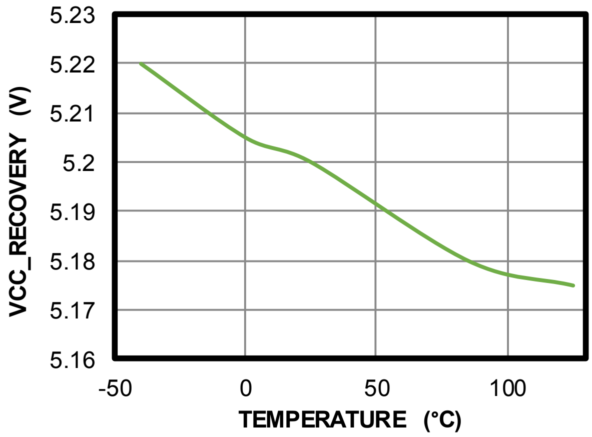


TYPICAL CHARACTERISTICS *(continued)*

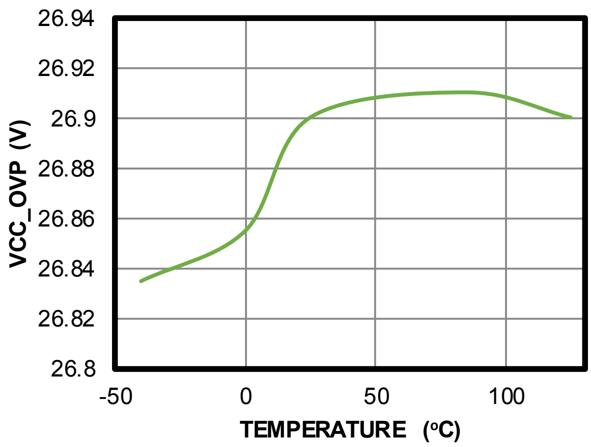
VCC_OFF vs. Temperature Chart



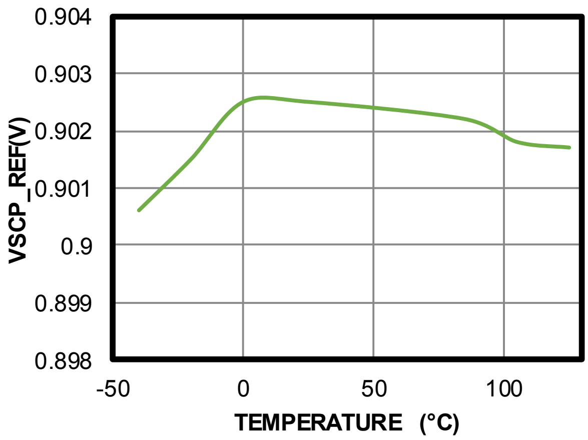
VCC_Recovery vs. Temperature Chart



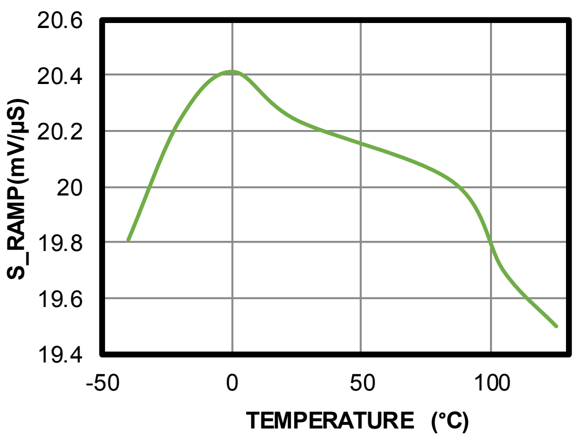
VCC_OVP vs. Temperature Chart



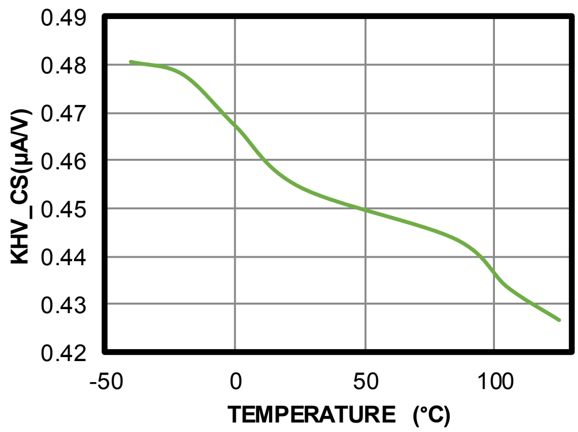
VSCP_REF vs. Temperature Chart



S_RAMP vs. Temperature Chart

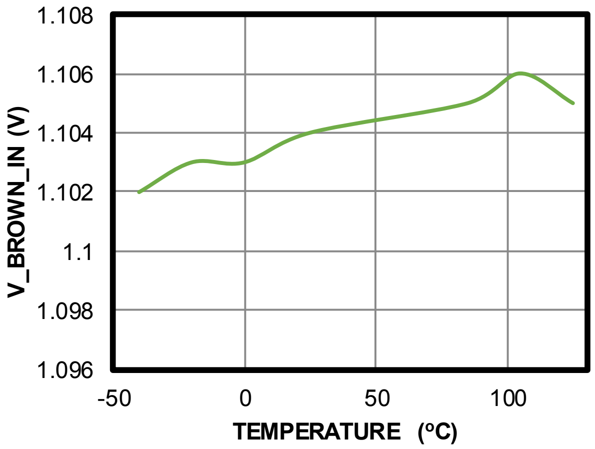


KHV_CS vs. Temperature Chart

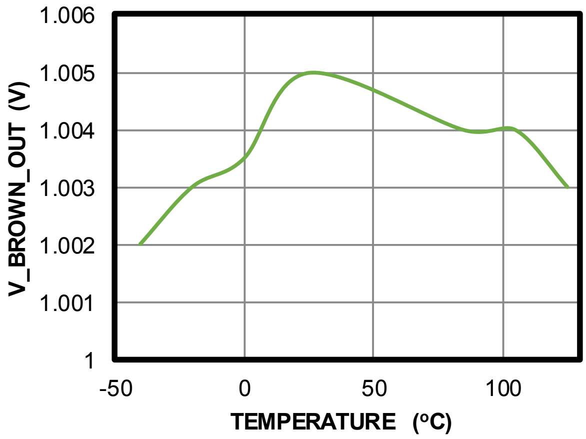


TYPICAL CHARACTERISTICS *(continued)*

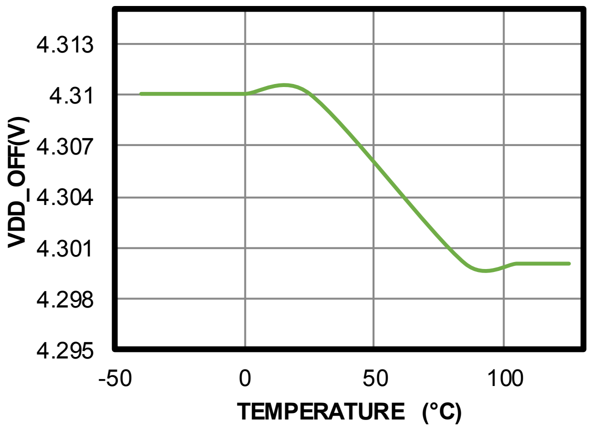
V_Brown_In vs. Temperature Chart



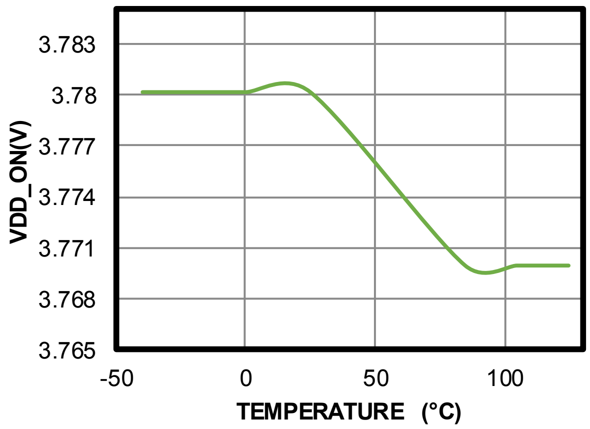
V_Brown_Out vs. Temperature Chart



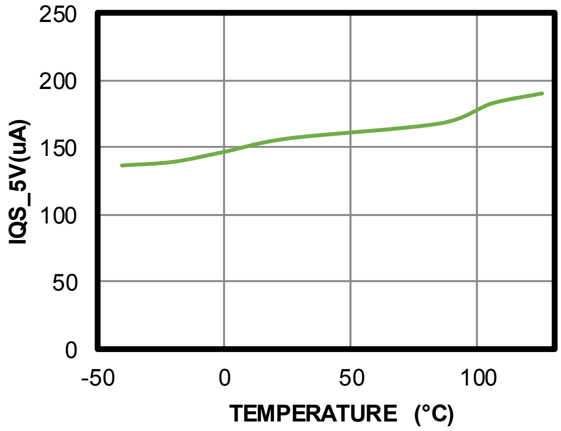
VDD_OFF vs. Temperature Chart



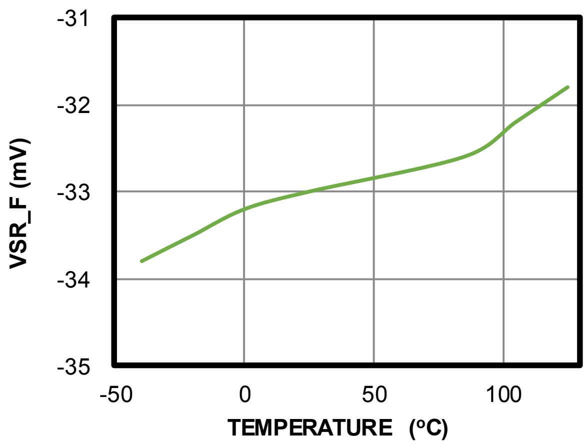
VDD_ON vs. Temperature Chart



IQS_5V vs. Temperature Chart

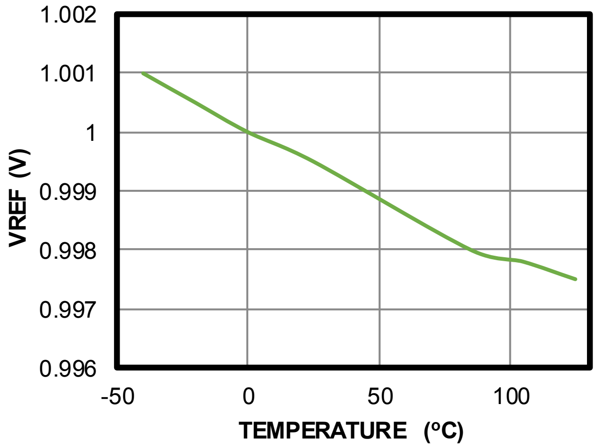


VSR_F vs. Temperature Chart

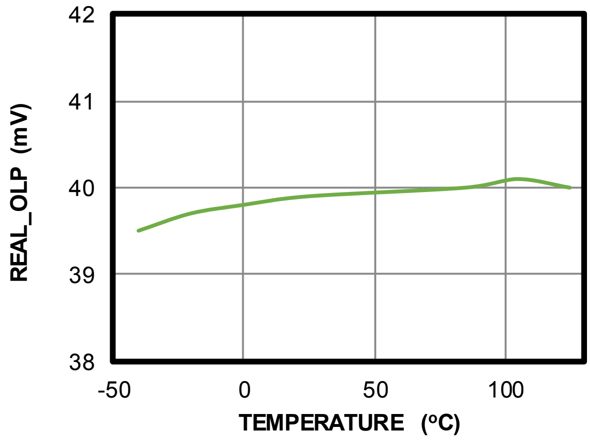


TYPICAL CHARACTERISTICS *(continued)*

VREF vs. Temperature Chart



Real_OLP vs. Temperature Chart

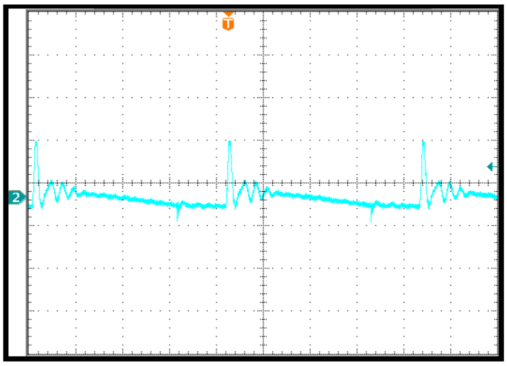


TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 110V_{AC}, V_{OUT} = 12V, I_{OUT} = 5A, unless otherwise noted.

Output Ripple
Full Load

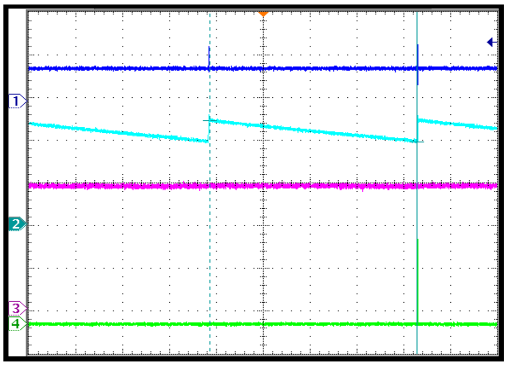
CH2: V_{OUT_AC} 200mV/div.



4μs/div.

Steady State
No Load

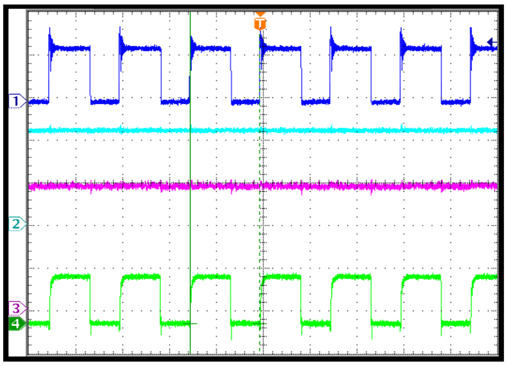
CH1: V_{DS} 200V/div.
CH2: V_{CC} 5V/div.
CH3: V_{OUT} 4V/div.
CH4: V_{SR} 5V/div.



100ms/div.

Steady State
Full Load

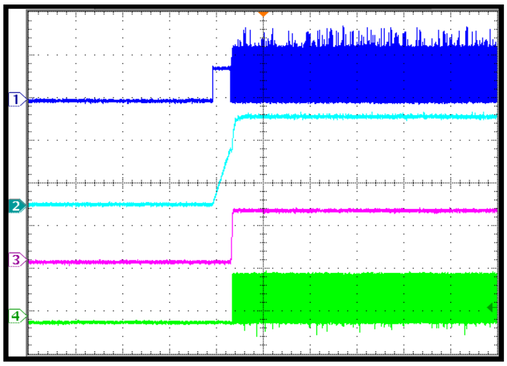
CH1: V_{DS} 200V/div.
CH2: V_{CC} 10V/div.
CH3: V_{OUT} 4V/div.
CH4: V_{SR} 10V/div.



10μs/div.

Start-Up
Full Load

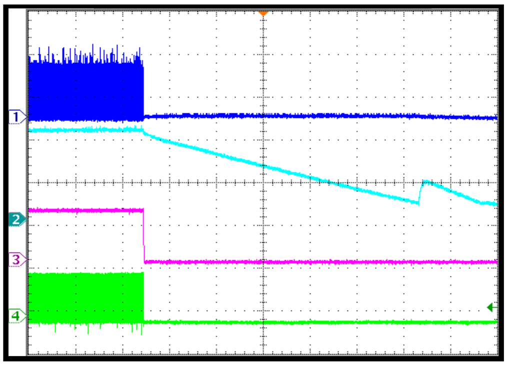
CH1: V_{DS} 200V/div.
CH2: V_{CC} 10V/div.
CH3: V_{OUT} 10V/div.
CH4: V_{SR} 10V/div.



400ms/div.

Shutdown
Full Load

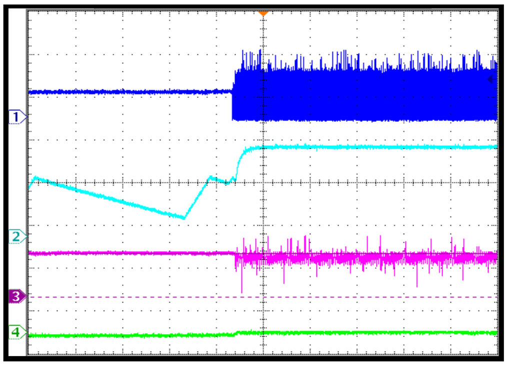
CH1: V_{DS} 200V/div.
CH2: V_{CC} 10V/div.
CH3: V_{OUT} 10V/div.
CH4: V_{SR} 10V/div.



1s/div.

External B/I
Full Load

CH1: V_{DS} 200V/div.
CH2: V_{CC} 10V/div.
CH3: V_{EBO} 1V/div.



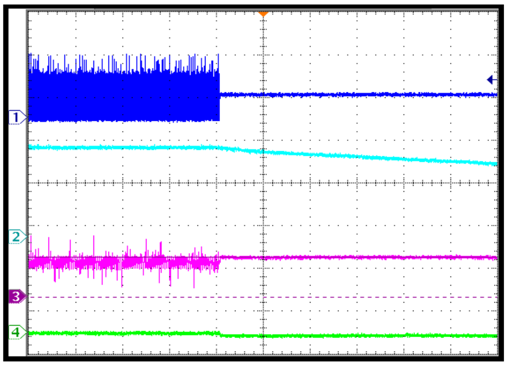
200ms/div.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 110V_{AC}, V_{OUT} = 12V, I_{OUT} = 5A, unless otherwise noted.

External B/O
Full Load

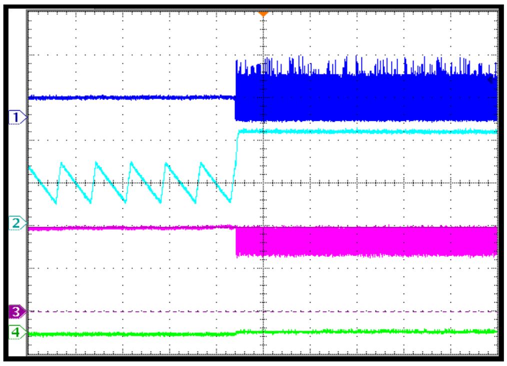
CH1: V_{DS} 200V/div.
CH2: V_{CC} 10V/div.
CH3: V_{EBO} 1V/div.



200ms/div.

Internal B/I
Full Load

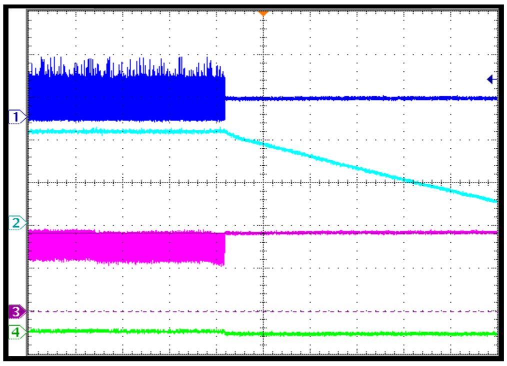
CH1: V_{DS} 200V/div.
CH2: V_{CC} 10V/div.
CH3: V_{HV} 50V/div.



1s/div.

Internal B/O
Full Load

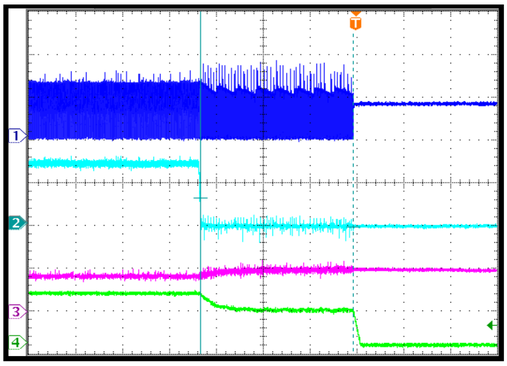
CH1: V_{DS} 200V/div.
CH2: V_{CC} 10V/div.
CH3: V_{HV} 50V/div.



1s/div.

OLP by COMP
Full Load

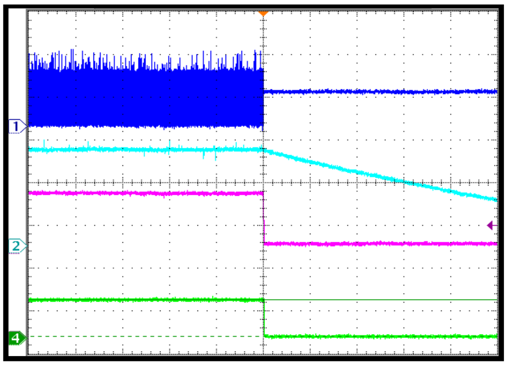
CH1: V_{DS} 200V/div.
CH2: V_{COMP} 1V/div.
CH3: V_{CC} 20V/div.
CH4: V_{OUT} 10V/div.



20ms/div.

OLP by IS
Full Load

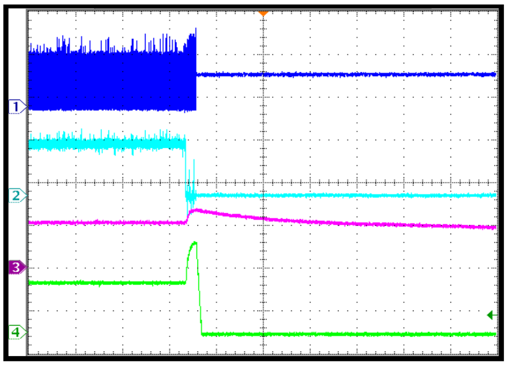
CH1: V_{DS} 200V/div.
CH2: V_{CC} 10V/div.
CH3: V_{OUT} 10V/div.
CH4: I_{OUT} 5A/div.



400ms/div.

OVP
Full Load

CH1: V_{DS} 200V/div.
CH2: V_{COMP} 1V/div.
CH3: V_{CC} 20V/div.
CH4: V_{OUT} 10V/div.



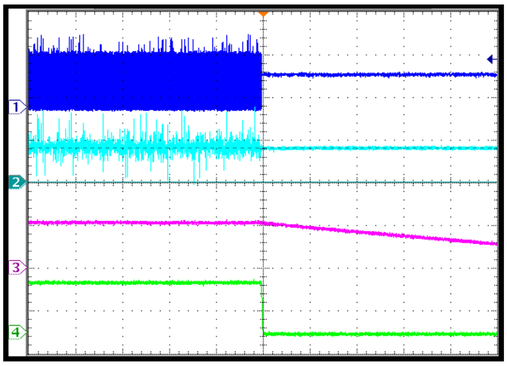
200ms/div.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 110V_{AC}, V_{OUT} = 12V, I_{OUT} = 5A, unless otherwise noted.

PEP Entry

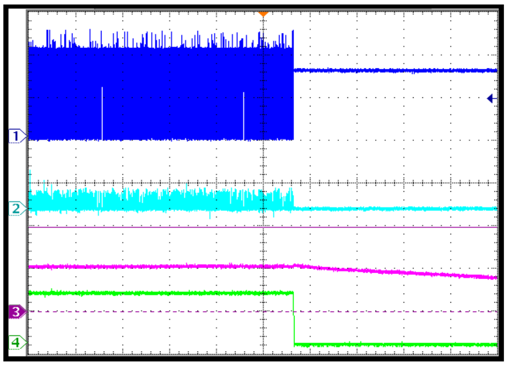
Full Load



400ms/div.

SCP Entry

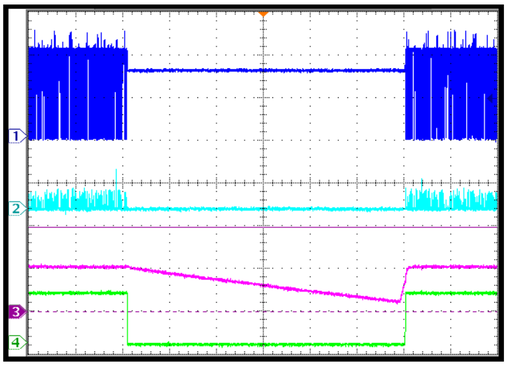
V_{IN} = 220V_{AC}, Full Load



400ms/div.

SCP Recovery

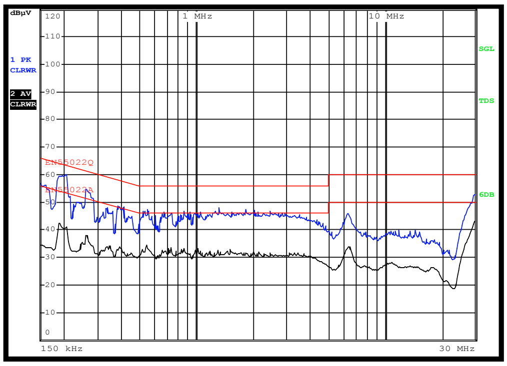
V_{IN} = 220V_{AC}, Full Load



1s/div.

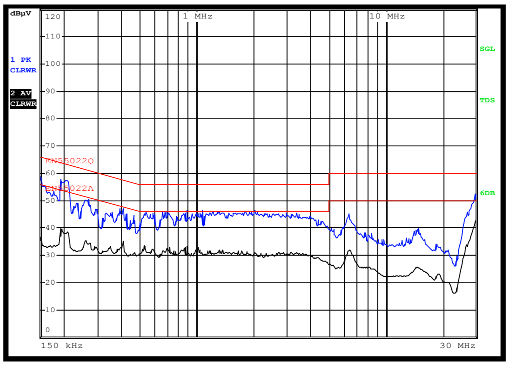
EMI

110L, Full Load



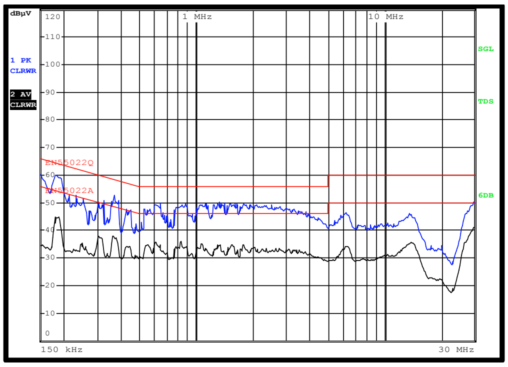
EMI

110N, Full Load



EMI

220L, Full Load

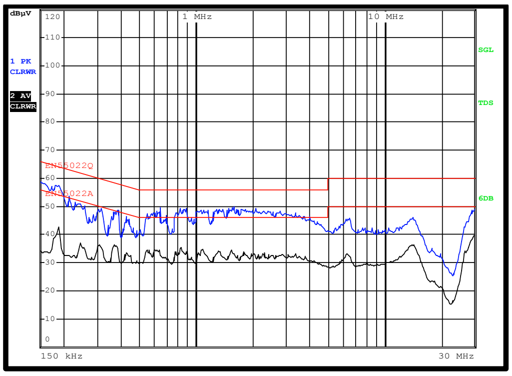


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

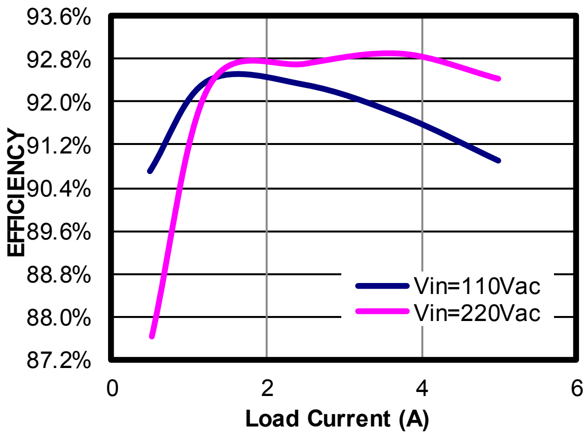
V_{IN} = 110V_{AC}, V_{OUT} = 12V, I_{OUT} = 5A, unless otherwise noted.

EMI

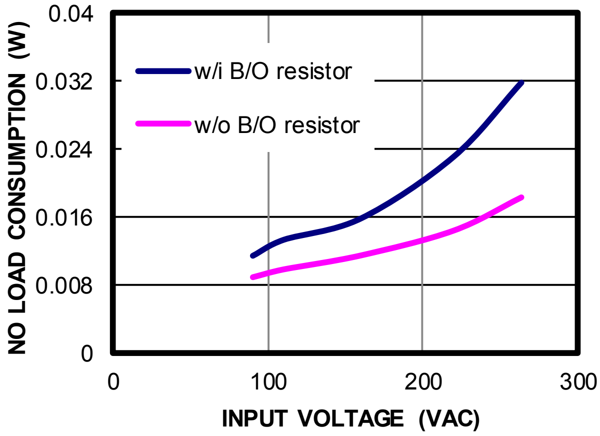
220N, Full Load



Efficiency vs. Load Current



No-Load Consumption vs. Input Voltage



		4-Point Average Efficiency	10% Load Efficiency	No-Load Consumption (W)
DoE Level VI		0.88	--	0.21
CoC V5	Tier 1	0.89	0.79	0.25
	Tier 2	0.89	0.79	0.15
Test Data	V_{IN} = 110V_{AC}	0.918	0.907	0.013 (2*5.1MΩ B/O resistor) 0.010 (internal B/O)
	V_{IN} = 200V_{AC}	0.925	0.876	0.023 (2*5.1MΩ B/O resistor) 0.014 (internal B/O)

PIN FUNCTIONS

Pin # -GY	Pin # -GYE	Name	Description
1	1	PEP	**External protection on the primary side.** Protections include, but are not limited to, over-temperature protection (OTP) for the primary MOSFET and over-voltage protection (OVP) on the auxiliary winding. An internal current source allows for a direct connection.
2	2	PGND	**Ground of the primary-side IC.**
3	3	PVB	**Primary voltage bypass.** An external ceramic capacitor (typically 1µF/6.3V) can be connected to PVB.
4	4	CS	**Primary MOSFET current sense for peak-current mode regulation and SCP function.** CS also implements over-power consumption based on the HV voltage.
5	5	VCC	**Power supply for the primary IC operation.** VCC senses the output voltage indirectly to achieve OVP.
6	6	PDrv	**Output drive for the external power MOSFET.**
7	7	PGND	**Ground of the primary side IC.**
8	8	EBO	**Input sense.** EBO is connected to external dividing resistors to sense the input voltage. This provides a more accurate brown-in/-out and an adjustable threshold. EBO is shorted to PGND to disable the external sensing. This way, brown-in/-out relies on internal sensing through HV.
9		NC	**No connection.**
10	10	HV	**High voltage.** HV implements an internal high-voltage current source for the primary IC start-up and normal operation. HV samples the input voltage for brown-in/-out and line compensation on the primary-peak current.
11	11	SRD	**Drain voltage sense of the synchronous rectifying MOSFET.**
12	12	SDrv	**Output drive for the external power MOSFET.**
13	13	SVB	**Secondary voltage bypass.** An external ceramic capacitor (typically 1µF/6.3V) can be connected to SVB.
14	14	SGND	**Ground of the secondary side.**
15	15	COMP	**Internal error amplifier for output voltage regulation.** Connect the compensation network to COMP to adjust the regulating performance.
16	16	CP	**Output cable drop compensation.** A 1µF ceramic capacitor can be connected to CP as a low-pass filter. The compensation voltage can be adjusted by parallel resistors. Short CP to SGND directly if CP is not needed.
17	17	VDD	**Power supply for the secondary IC operation and external MOSFET driving.**
18	18	FB	**Feedback for the constant voltage regulation.** Connect FB to dividing resistors to sense the output voltage.
19	19	IS	**Overload protection sense.** IS senses OLP by connecting a current sensing resistor in the output loop.
20	20	SGND	**Ground of the secondary side.**

BLOCK DIAGRAM

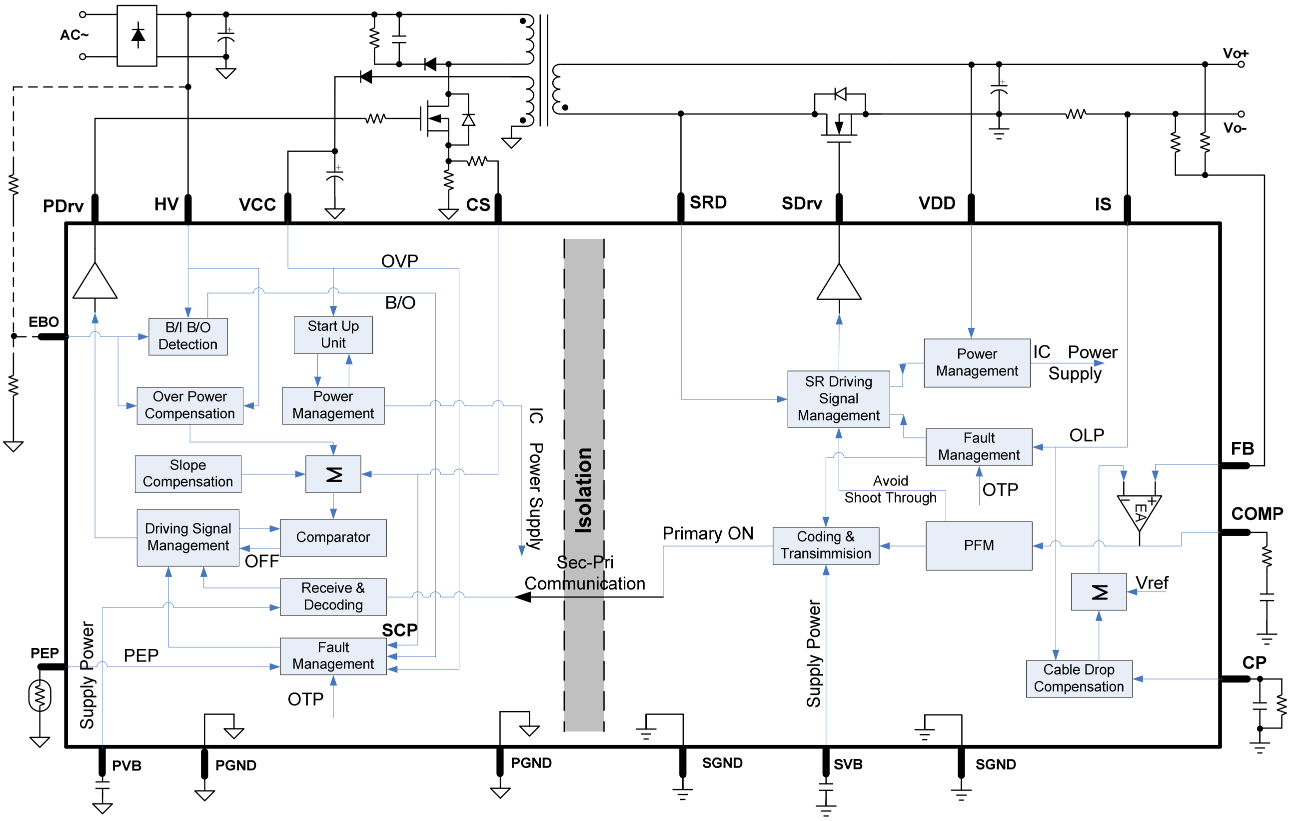


Figure 1: Functional Block Diagram

OPERATION

The MPX2001 is an all-in-one flyback controller that maintains all benefits of a secondary-side regulator (SSRs), reducing system complexity and the total solution cost. The MPX2001 solution implements a complete secondary-side regulation scheme. Both the control loop and the modulation block are placed on the secondary side, so the drive signal of the synchronous rectifier (SR) can be perfectly matched with the drive signal of the primary-side MOSFET. With this feature, the SR is able to operate safely in continuous conduction mode (CCM), which helps increase overall efficiency greatly and provide more flexibility to the design.

PRIMARY IC FUNCTION SECTION

Self-Configuration at Start-Up

Once VCC is higher than the minimum operation voltage (V_{CC-MIN}) (typically 8V), the primary IC starts to read the EBO configuration. This is done before entering any other operation.

If EBO is connected to an external resistor divider (typically >1kΩ), the external brown-in/-out mode is selected. In this mode, the brown-in/-out function senses the input voltage through EBO instead of sensing it through HV internally. The brown-in/-out detection is always enabled, regardless of whether the HV current source is turned on or off. This mode provides a more accurate brown-in/-out approach and adjustable thresholds.

If EBO is shorted to PGND to disable the external sensing, the internal brown-in/-out mode is selected. In this mode, brown-in/-out relies on the internal sensing through HV. Brown-in/-out detection turns off when the HV current source is turned on (to avoid the effect of the HV voltage drop) and is always turned back on after the HV current source is turned off.

This self-configuration action is executed only once, and the results are latched as long as the primary IC is active.

Start-Up with Brown-In/-Out Detection

Initially, all primary IC operation is disabled when there is no power applied, and the brown-in/-out flag defaults in brown-out state. The VCC of primary IC (VCC) is charged up by the internal high-voltage current source drawn from HV. The current source is turned off once VCC reaches $V_{CC-IOFF}$ (typically 14.5V).

If the device is configured with external brown-in/-out mode, brown-in/-out detection is enabled right after self-configuration. If the device is configured with brown-in/-out internal mode, brown-in/-out is only enabled after the HV current source is turned off. If the HV voltage is higher than V_{HV-ON} (typically 106V), then this is treated as a brown-in condition. The primary IC turns on the HV current source to charge VCC back to $V_{CC-IOFF}$ (to guarantee a maximized start-up window) and operates in normal start-up mode. Otherwise, it is treated as a brown-out protection condition. The primary IC operation remains disabled until VCC drops down to V_{CC-AUT} (typically 5.3V), and VCC is charged up by the high-voltage current source all over again.

Once VCC is higher than the minimum operation voltage (V_{CC-MIN}), the primary IC begins monitoring on the sync signal transmitted through the insulation channel. Before brown-in is detected and the primary IC runs into normal start-up mode, the primary IC can already determine what status the secondary IC is in. As shown in Figure 2, there are three conditions for primary IC start-up.

1. If there is no logic high state detected for the sync signal, the primary IC indicates that either the secondary IC is out of power or the system is recovering from a fault state. In this case, when brown-in is detected and the primary IC runs in normal start-up mode, the primary IC starts switching on its own with the maximum switching frequency and the maximum peak current. Once any logic-high state of the sync signal is detected, the primary IC stops independent switching, and the secondary IC takes control. There is also a time limit on the primary start-up period. Even if there is no logic-high state detected for the sync signal, the independent primary switching stops when the timer (t_{OCP}) times out. This means that there is a fault condition present, such as overload, which is preventing the secondary IC from powering up successfully. t_{OCP} starts after the soft-start period. Once the primary

OCP flag is set, and the primary IC runs in a protection mode.

2. If a normal sync signal is detected before the primary IC enters start-up mode, the primary IC does not require independent switching. The primary IC follows the sync modulation right after brown-in is detected.
3. If any sync signal is detected before start-up, the IC indicates a fault condition, such as overload on the secondary side. In this case, the primary IC does not switch at all, but sets the protection flag and runs in a protection mode.

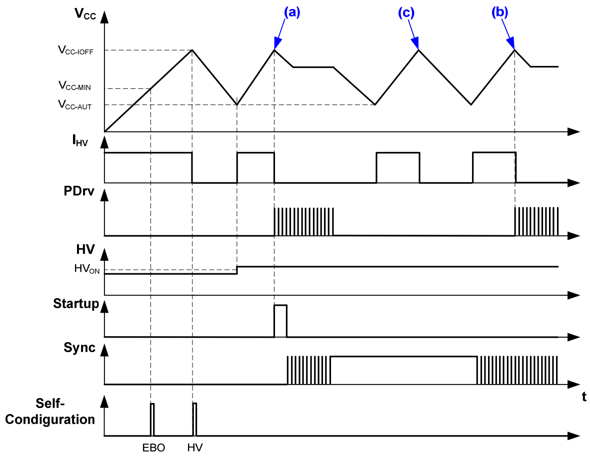


Figure 2: Start-Up Logic for Primary IC

Brown-Out Protection during Normal Operation

To prevent any unwanted behavior from the power supply caused by an insufficient input voltage, the primary IC implements brown-out protection. When the HV voltage is lower than V_{HV-OFF} (typically 96V, internal B/O) or the EBO voltage is lower than $V_{EBO-OFF}$ (typically 1V, external B/O), the brown-out timer starts running. Conversely, whenever the HV voltage is higher than V_{HV-OFF} or the EBO voltage is higher than V_{EBO_OFF}, the timer is reset. If the brown-out timer is over t_{BO}, the primary IC enters brown-out protection, and VCC enters hiccup operation between V_{CC-AUT} (typically 5.3V) and $V_{CC-IOFF}$ (typically 14.5V). The primary IC does not start up again until there is a valid brown-in detection.

If brown-in/-out relies on internal sensing through HV, the brown-in/-out detection always pauses when the HV current source is turned on (to avoid the effect of the HV voltage drop) and resumes after the HV current source is turned off.

Soft Start (SS)

To reduce stress on the power circuits, a soft-start function is implemented in the primary IC. When the primary IC enters normal start-up mode and starts switching on its own, the internal soft start increases the current limit from $V_{IPK-Min}$ (typically 0.15V) to $V_{IPK-Max}$ (typically 0.6V) and the switching frequency from f_{S-Soft} (typically 20kHz) to f_{S-Max} (typically 85kHz). The duration of the soft-start period is t_{Soft} (typically 10ms).

Peak-Current Control with Internal Slope Compensation

The primary IC employs peak-current-mode control with an on time controlled by comparing the voltage across the CS, current sense resistor with the internal reference. The reference voltage is controlled by the sync frequency with a maximum value of $V_{IPK-Max}$ and a minimum value of $V_{IPK-Min}$. The reference voltage is clamped at $V_{IPK-Max}$ when the sync frequency is higher than f_{Sync-H} (typically 42kHz) and is clamped at $V_{IPK-Min}$ when the sync frequency is lower than f_{Sync-L} (typically 20kHz) (see Figure 3). When the sync frequency is between f_{Sync-H} and f_{Sync-L}, the reference is adjusted proportionately.

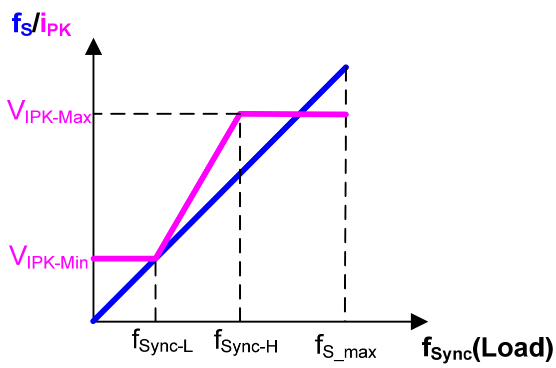


Figure 3: Peak-Current Reference vs. Sync Frequency

A synchronized positive slope is added to the sensed current signal on CS to prevent subharmonic oscillation and guarantee stable peak-current mode control over a wide range of input voltages. The compensation is proportionately reduced as the peak current decreases.

Due to the parasitic capacitance, a spike usually occurs on the sensing resistor after the MOSFET is turned on. To prevent the peak-current limitation comparator from being falsely triggered by this turn-on spike, a leading edge blanking (LEB) function is implemented on the comparator. During the blanking time, the comparator for peak-current limitation is disabled, so the MOSFET cannot be turned off. Two-level LEB is adopted in the comparator. Normal operation has t_{LEB_L} (typically 276ns) and t_{LEB_S} (typically 235ns) for SCP.

Line Compensation for Peak-Current Control

Ideally, in peak-current-mode control, the primary peak current should be exactly the same as the reference because of the peak-current control operation. However, due to the logic propagation delay and driver delay, the actual peak current is always higher than the reference value. Moreover, the difference between the actual value and reference value varies with the input voltage. A higher input voltage results in a larger error of the peak current (see Figure 4). This leads to a significant variation in the maximum power limitation.

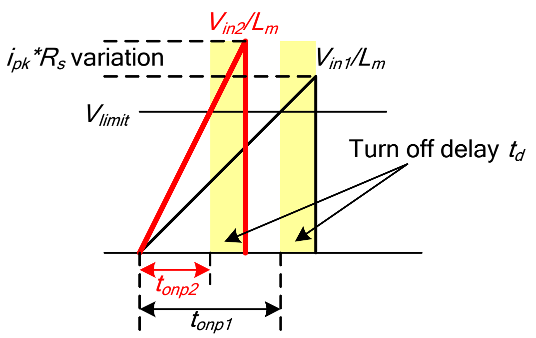


Figure 4: Peak Current Difference Caused by Turn-Off Delay

To compensate for this variation and improve overload protection (OLP) accuracy, an offset proportional to the input voltage is added on the CS signal. The offset is created by an internal sourcing current on CS flowing across an external resistor (R_{HVCS}), and the current source is proportional to the HV voltage (see Figure 5). The compensation level can be adjusted by R_{HVCS} externally.

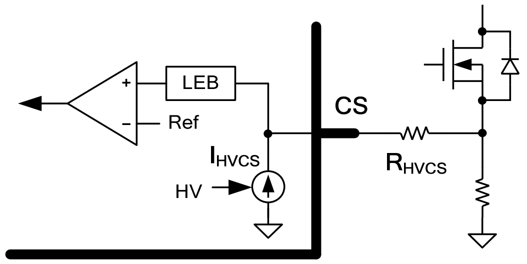


Figure 5: Implementation of Line Compensation Function

The compensation current is applied completely only when the peak current reference is at its maximum limit. This compensation current is disabled when the peak current reference is lower than 90% of the maximum value (see Figure 6).

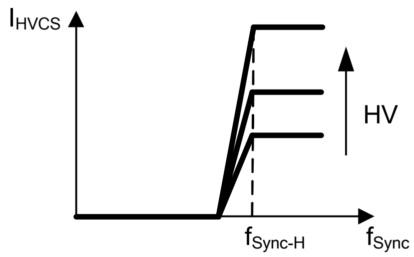


Figure 6: Current on CS for Line Compensation

Driver

The driver capability is specified in the Electrical Characteristics table on page 5. The voltage is clamped internally at V_{Clamp} (typically 11.5V) to guarantee safe operation of the external MOSFET.

Under-Voltage Lockout (UVLO)

UVLO stops the primary switching whenever VCC is under $V_{CC\text{-}MIN}$ (typically 8V). The HV current source is enabled when VCC is under $V_{CC\text{-}AUT}$ (typically 5.3V).

Protections

The primary IC provides full protection features as well as solid response to the secondary IC protections. Primary protections are all implemented as either auto-restart mode or latch-off mode. When a protection is triggered, the switching is terminated immediately, and VCC drops. Once VCC drops to $V_{CC\text{-}AUT}$, the related protection flag is reset, and the HV current source is enabled to charge the VCC capacitor. Then the primary IC enters normal start-up mode.

Short-Circuit Protection (SCP)

If the CS voltage is over V_{SCP}, the peak current is not well-controlled by the peak-current limitation due to a fault condition, such as winding short-circuit or output short-circuit. Short-circuit protection (SCP) is triggered as an auto-restart mode protection. A reduced LEB time (t_{LEB-S}, typically 235ns) is also adopted by the SCP comparator.

Over-Voltage Protection (OVP)

If VCC is over V_{CC-OVP} (typically 27V), it indicates that the output voltage is not under control, and a large output overshoot can occur. OVP is triggered as a result in an auto-restart mode. The primary OVP can avoid component breakdown caused by over-stress.

Brown-Out Protection (BOP)

For more information about brown-out protection, refer to the Start-Up with Brown-In/-Out Detection section on page 18 and the Brown-Out Protection during Normal Operation section on page 19. Brown-out protection (BOP) is an auto-restart mode protection.

Primary Over-Temperature Protection (POTP)

To prevent any thermal damage on the chip, primary over-temperature protection (POTP) shuts down the switching immediately when the junction temperature is over T_{OTP} (typically 150°C). The protection flag is latched until the junction temperature drops by T_{Δ} (typically 40°C), and POTP enters auto-restart mode.

Primary Over-Current Protection (POCP)

For more information about primary over-current protection (POCP), refer to the Start-Up with Brown-In/-Out Detection section on page 18. If the primary side does not receive a start-up signal from the secondary side for t_{OCP} (typically 69ms), primary over-current protection is triggered. POCP is an auto-restart mode protection.

Open/Short Protection on CS (CSP)

CS is pulled high internally by the line compensation current source. SCP is triggered if CS is open. Conversely, CSP can also be triggered if the duty-on time reaches ~10µs and the CS voltage is ~0V, or the IC indicates a short-circuit condition on the current-sensing resistor or an inappropriate transformer design. CSP is an auto-restart mode protection.

Primary External Protection (PEP)

PEP is a general-purpose protection pin. There is an internal current soured out of PEP with a fixed value of I_{PEP} (typically 100µA) (see Figure 7). A resistor or a BJT can be connected to PEP to create the target voltage. When the PEP voltage is lower than the protection trigger threshold (V_{PEP-T}, typically 0.5V) and the condition lasts longer than the trigger delay time (t_{PEP_T}, typically 300µs), the sync signal is set to logic high by PEP. The PEP flag is not reset until VCC drops below V_{CC-AUT}.

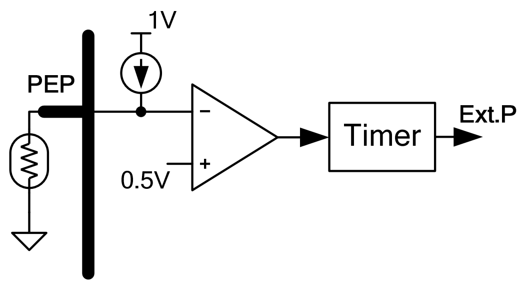


Figure 7: Primary External Protection

PEP also has a saturation voltage (V_{PEP-S}, typically 1V). If the external resistor is high enough to make the PEP voltage reach the saturation value, the PEP current is no longer fixed, but determined by the external resistance. Due to this characteristic, the current consumption during normal operation can be limited at a very low level.

Typically, PEP can be used to implement an OTP function for external power devices (e.g.: primary MOSFET) by connecting to a negative temperature coefficient (NTC) resistor.

Response to the Secondary Protections

For more information about responses to secondary protections, refer to the Start-Up with Brown-In/-Out Detection section on page 18.

SECONDARY IC FUNCTION SECTION

Self-Configuration at Start-Up

As soon as the VDD voltage is higher than the minimum operating voltage (V_{DD-ON}, typically 4.3V), the secondary IC begins a self-configuration procedure before entering any other operation.

If there is a capacitance (typically ≥1μF) on CP, the CP (cable drop compensation) function is enabled. The minimal PFM frequency default is 20kHz. Short CP to SGND if cable drop compensation is not needed.

Synchronous Rectifier, Normal Operation

After the primary-side MOSFET is turned off, the inductor current commutates from the primary side to the secondary side, which makes the drain voltage of the SR MOSFET drop. Once the voltage on SRD pin crosses zero, the secondary chip starts to set the SR driver, and the SR MOSFET is turned on after a turn-on delay (see Figure 8). During the minimum ON time, the turn-off action is not blanked completely, but only the turn-off threshold is increased to $V_{SR-OFF2}$. This ensures that the part can always be turned off, even during the turn-on blanking period.

During the SR conduction period, the gate voltage is regulated based on the forward-voltage drop across the MOSFET (V_{SRD}). When V_{SRD} is lower than the internal reference voltage (V_{SR-F}, typically -33mV), the gate driver is turned on fully to obtain a minimal on state resistance. Voltage across the SR MOSFET V_{SRD} rises as the current decreases. When V_{SRD} is close to or less negative than V_{SR-F}, the gate voltage is linearly reduced to increase the on state resistance. In this way, the change in V_{SRD} is minimized and kept roughly flat. This feature prevents a premature turn-off and effectively maximizes the SR conduction period.

As V_{SRD} continues to rise until it crosses the voltage threshold, the gate is turned off after a very short turn-off delay. This regulating behavior during the SR conduction period also helps reduce the turn-off delay since the gate voltage was already low before turn off.

After the SR MOSFET is turned off, SR operation is disabled to prevent any unexpected turn-on for at least 300ns until the next sync signal pulse. This minimal off-logic is only valid for discontinuous conduction mode (DCM) operation when the SR drive is turned off before the sync signal comes. The SR turn-on logic recovers after a delay time from the sync rising edge and waits for another zero crossing of V_{SRD}.

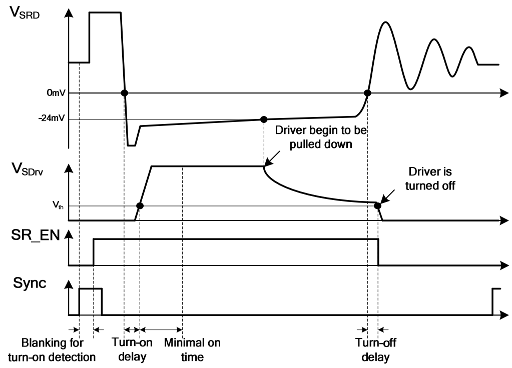


Figure 8: Synchronous Rectifying Operation

Synchronous Rectifier, CCM Operation, Light-Load Operation

The SR gate driver is turned off at the rising edge of the internal sync signal. As a result, the chip is able to support reliable CCM operation. If the SR drive is turned off by the sync signal in CCM operation, the SR is turned off for at least 300ns. Then the turn-on logic does not recover until the drain voltage is higher than 1.6V. To improve light-load efficiency and reduce no-load power consumption, the SR driver is disabled when the IC enters burst mode. Although the SR driver is disabled, the control logic still works. Once the IC exits burst mode, the SR driver recovers.

Output Voltage Regulation

The output voltage is sensed and fed back to FB using external resistor divider. The feedback voltage is compared with an internal precision voltage reference (V_{REF}, typically 1V) by internal error amplifier. The voltage difference is amplified by the transconductance (GM) and appears as a current source at COMP. The external compensation network can be configured at COMP to adjust the regulation performance. Since FB is connected to the non-inverting pin of the error amplifier, the COMP voltage is in phase and proportional to the output voltage and inversely proportional to the load current (i.e.: the COMP voltage rises as the load current decreases). The COMP voltage is sent to the pulse-frequency modulation (PFM) block to modulate the sync frequency. A higher COMP voltage results in a lower sync frequency (see Figure 9) and therefore lower switching frequency, fs. The sync signal that carries all load information is then transmitted to the primary-side IC through the isolator. In this way, closed-loop regulation is achieved.

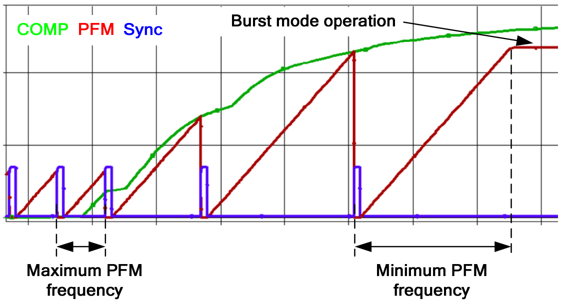


Figure 9: PFM Operation

The PFM frequency has maximum and minimum limitations. Regardless of how low or high the COMP voltage is, the maximal PFM frequency is limited at f_{s_max} (typically 85kHz), so the switching behavior of the sync signal is always guaranteed, and any damage from unexpected high switching frequencies can be prevented as well. However, when the COMP voltage rises above V_{Burst}, the modulation enters burst operation mode, so the minimal PFM frequency is limited by V_{Burst}.

Cable Drop Compensation

The compensation voltage is directly proportional to the voltage on IS. The external capacitor and resistor on CP are still used for filtering and voltage adjustment respectively.

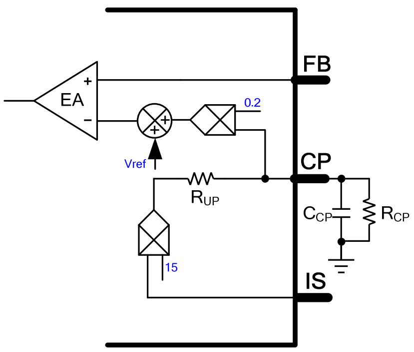


Figure 10: Cable Drop Compensation

PROTECTIONS

Secondary Under-Voltage Lockout (SUVLO)

The secondary IC does not begin operation until VDD rises above $V_{DD\text{-}ON}$ (typically 4.3V). When VDD falls below $V_{DD\text{-}OFF}$ (typically 3.8V), the secondary IC powers off, and all internal signals are reset. To avoid nuisance UVLO lock out during any transient, the UVLO circuit waits for 10usecs before generating a lock out command.

Secondary Overload Protection (SOLP)

Secondary overload protection (SOLP) can be achieved by connecting a current-sense resistor to IS. When the IS voltage is higher than the overload protection threshold (V_{OLP}, typically 40mV) and lasts longer than the overload protection delay time (t_{OLP}, typically 68ms), the sync signal is set to a logic-low state by SOLP. The SOLP flag is reset when the VDD voltage drops under $V_{DD\text{-}OFF}$ (typically 3.8V).

Even if IS is shorted to SGND, the SOLP function is still available, but is not as accurate. SOLP is implemented based on the COMP signal. If the COMP voltage remains at zero (smaller than the threshold where the sync frequency is set at the maximum limit), the OLP timer also starts running and triggers SOLP once it times out.

Secondary Over-Temperature Protection (SOTP)

To prevent any thermal damage on the chip, SOTP shuts down switching when the junction temperature is over T_{OTP} (typically 150°C). The protection flag is latched until the junction temperature drops by T_{Δ} (typically 40°C), and then SOTP enters auto-restart mode.

APPLICATION INFORMATION

Selecting the VCC Capacitor

Figure 11 shows the start-up circuit. VCC is charged by HV first. When VCC reaches V_{CC_IOFF}, HV stops charging, and the IC starts operating. To guarantee a successful start-up, the output voltage should be set up before VCC drops to V_{CC_MIN}.

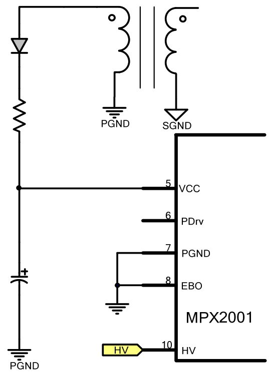


Figure 11: Start-Up Circuit

As a tradeoff between safe operation and cost for most applications, choose a VCC capacitor value around 22μF with Equation (1):

$$C_{VCC} > \frac{I_{OP} \cdot T_{Startup}}{VCC_{IOFF} - VCC_{MIN}} \tag{1}$$

Primary-Side Inductor Design (L_m)

The MPX2001 maximum switching frequency is recommended to be no higher than 80kHz. With internal slope compensation, the MPX2001 supports CCM when the duty cycle exceeds 50%. Set a ratio (K_P) of the primary inductor's ripple current amplitude vs. the peak current value to $0 < K_P \le 1$, where $K_P = 1$ for DCM (see Figure 12). A larger inductor leads to a smaller K_P, which can reduce RMS current, but increases transformer size. An optimal K_P value is between 0.6 and 0.8 for the universal input range and 0.8 to 1 for a $230V_{AC}$ input range.

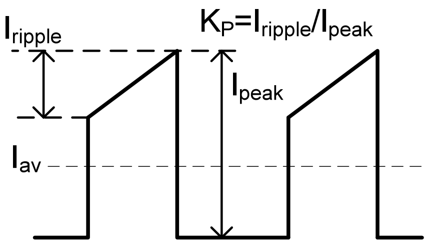


Figure 12: Typical Primary-Current Waveform

The input power (P_{in}) at the minimum input can be estimated with Equation (2):

$$P_{IN} = \frac{V_O \cdot I_O}{\eta} \tag{2}$$

Where V_O is the output voltage, I_O is the rated output current, and η is the estimated efficiency, generally between 0.85 and 0.9 depending on the input range and output application.

For CCM at a minimum input, the converter maximum duty cycle can be calculated with Equation (3):

$$D_{MAX} = \frac{(V_O + V_F) \cdot N}{(V_O + V_F) \cdot N + V_{in(min)}} \tag{3}$$

Where V_F is the secondary diode's forward voltage, N is the transformer turn ratio, and $V_{in(min)}$ is the minimum voltage on the bulk capacitor.

The MOSFET turn-on time can be calculated with Equation (4):

$$T_{on} = D \cdot T_s \tag{4}$$

Where T_s is the frequency jitter's dominant switching period, $\frac{1}{T_{smin}} = f_{smax} = 80kHz$.

The average, peak, ripple, and valley values of the primary current are calculated with Equation (5), Equation (6), Equation (7), and Equation (8):

$$I_{av} = \frac{P_{in}}{V_{in(min)}} \tag{5}$$

$$I_{peak} = \frac{I_{av}}{(1 - \frac{K_P}{2}) \cdot D} \tag{6}$$

$$I_{ripple} = K_P \cdot I_{peak} \tag{7}$$

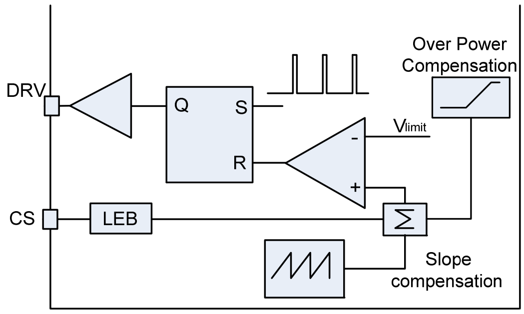
$$I_{valley} = (1 - K_P) \cdot I_{peak} \tag{8}$$

Estimate L_m with Equation (9):

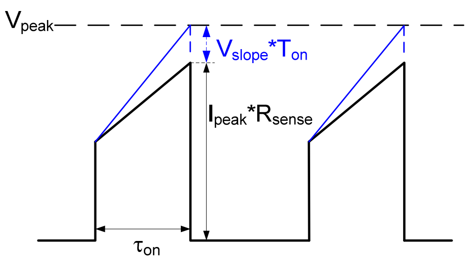
$$L_m = \frac{V_{in(min)} \cdot T_{on}}{I_{ripples}} \tag{9}$$

Current-Sense Resistor

Figure 13 shows the peak-current comparator logic and the subsequent waveform. When the sum of the sensing resistor voltage and the slope compensator reaches V_{peak}, the comparator goes high to reset the RS flip-flop, and DRV is pulled low to turn off the MOSFET. The maximum current limit (V_{limit}, as measured by V_{CS}) is 0.57V. The slope compensator (V_{slope}) is ~20mV/µs. At a low line, the over-power compensation is zero. Given a certain margin, use 0.95 x V_{limit} as V_{peak} at full load.



Peak-Current-Comparator Circuit



Typical Waveform

Figure 13: Peak-Current Comparator

Then the voltage on the sensing resistor can be obtained with Equation (10):

$$V_{sense} = 95\% \cdot V_{limit} - V_{slope} \cdot T_{on} \quad (10)$$

The value of the sense resistor can be calculated with Equation (11):

$$R_{sense} = \frac{V_{sense}}{I_{peak}} \quad (11)$$

Select the current sense resistor with an appropriate power rating. Calculate the sense resistor power loss with Equation (12):

$$P_{sense} = \left[\left(\frac{I_{peak} + I_{valley}}{2}\right)^2 + \frac{1}{12}\left(I_{peak} - I_{valley}\right)^2\right] \cdot D \cdot R_{sense} \quad (12)$$

Over-Power Consumption and Low-Pass Filter on CS

The MPX2001 uses an over-power compensation function (OPC) by drawing current from CS. OPC minimizes the OLP difference caused by different input voltages. The offset current is proportional to the input peak voltage sensed by HV.

Supposing the resistor in the current sensing loop is R_{opc} and the bus voltage is V_{HV}, calculate the compensation voltage on CS with Equation (13):

$$V_{comp} = R_{opc} \cdot I_{HVCS} \quad (13)$$

The compensation criterion is making the FB voltage in a full-load situation similar whether in high line or low line.

A small capacitor connected to CS with R_{opc} forms a low-pass filter for noise filtering when the MOSFET turns on and off (see Figure 14). The low-pass filter's R-C constant should not exceed a third of the leading-edge blanking period for SCP (T_{LEB-S}, typically 235ns). Otherwise, the filtered sensed voltage cannot reach the SCP point to trigger SCP if an output short circuit occurs.

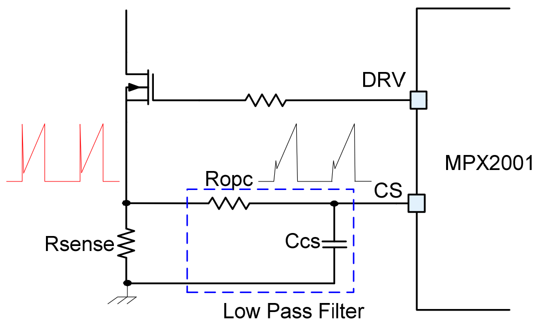


Figure 14: Low-Pass Filter on CS

Ramp Compensation

When adopting a peak-current control, subharmonic oscillations occur when D > 0.5 in CCM. The MPX2001 is equipped with internal ramp compensation to solve this problem. α is calculated with Equation (14):

$$\alpha = \frac{\frac{D_{max} \cdot V_{in(min)}}{(1-D_{max}) \cdot L_m} \cdot R_{sense} - m_a}{\frac{V_{in(min)}}{L_m} \cdot R_{sense} + m_a} \quad (14)$$

Where m_a is the minimum internal slope value of the compensation ramp (18mV/µs), $\frac{V_{in(min)}}{L_m} \cdot R_{sense}$ is the slew rate of the primary-side voltage sensed by a CS resistor, $\frac{D_{max} \cdot V_{in(min)}}{(1-D_{max}) \cdot L_m} \cdot R_{sense}$ is the slew rate of the equivalent secondary-side voltage sensed by CS resistor respectively. For stable operation, α must be less than 1.

External Protection through PEP

PEP can be used to implement an OTP function for external power devices (e.g.: primary MOSFET) by connecting an NTC resistor to PEP (see Figure 15). PEP can also be used to implement an OVP function by connecting several passive components to PEP (see Figure 17).

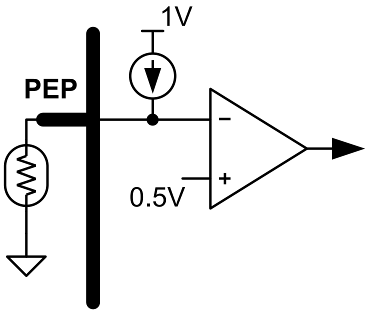


Figure 15: OTP through PEP

The sourcing current of PEP is I_{PEP} (typically 100µA). The resistance of the NTC resistor at a working temperature should satisfy Equation (15):

$$I_{PEP} * R_{PEP} > V_{PEP\text{-}T} \quad (15)$$

When the temperature increases, the resistance of the NTC resistor decreases. Figure 16 shows the typical waveform of NTC resistance vs. temperature.

At a protected temperature, the resistance satisfies Equation (16):

$$I_{PEP} * R_{PEP} < V_{PEP-T} \quad (16)$$

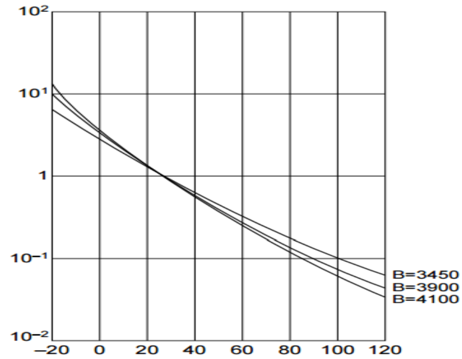


Figure 16: NTC Resistance vs. Temperature

The OVP can also be configured by PEP. The breakdown voltage (BV) of the Zener diode should be the VCC voltage when a secondary over-voltage condition occurs.

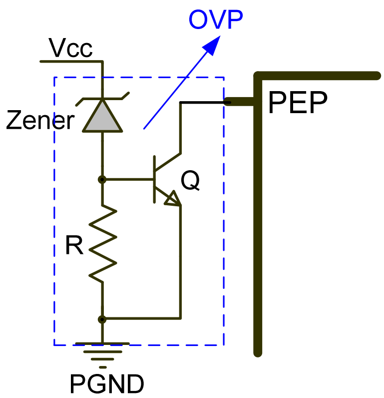


Figure 17: OVP through PEP

Cable-Drop Compensation

As described in Figure 10, the CP voltage is proportional to the IS voltage. The IS voltage increases 15 times on CP. Then the voltage on CP is multiplied by 0.2 and is added to V_{REF} (typically 1V) to compare with V_{FB}. One 1µF ceramic capacitor is recommended on CP. The CP voltage can be adjusted by connecting a resistor to CP. Calculate the CP voltage with Equation (17):

$$V_{CP} = V_{IS} * 15 * \frac{R_{CP}}{(200k + R_{CP})} \quad (17)$$

The offset voltage on the reference can be calculated with Equation (18):

$$V_{REF\_OFFSET} = 0.2 * V_{CP} \quad (18)$$

SR MOSFET Selection

Power MOSFET selection is a trade-off between the $R_{DS(ON)}$ and Qg. To achieve higher efficiency, a MOSFET with a smaller $R_{DS(ON)}$ is recommended. Typically, Qg is larger when the $R_{DS(ON)}$ is smaller, which makes the turn-on/off speed lower and leads to a larger power loss and driver loss. Additionally, the gate driving signal may turn off prematurely with an improper Qg SR MOSFET. Because V_{DS} is adjusted at about -33mV during the driving period (when the switching current is fairly small), a MOSFET with too low $R_{DS(ON)}$ value is not recommended because the gate driver is pulled low when $V_{DS} = -I_{SD} \times R_{DS(ON)}$ is larger than -33mV. The $R_{DS(ON)}$ of the MOSFET does not contribute to conduction loss. The conduction loss is $P_{CON} = -V_{DS} \times I_{SD} \approx I_{SD} \times 33mV$.

Figure 18 shows the typical waveform of a QR flyback. Assuming a 50% duty cycle, the output current is I_{OUT}.

To achieve a fairly high use of the MOSFET's $R_{DS(ON)}$, the MOSFET should be turned on completely for at least 50% of the SR conduction period. Calculate V_{DS} with Equation (19):

$$V_{DS} = -I_C \times R_{ON} = -2 \times I_{OUT} \times R_{ON} \leq -V_{FWD} \quad (19)$$

Where V_{DS} is the drain source voltage of the MOSFET, and V_{FWD} is the forward voltage threshold (~33mV).

The MOSFET's $R_{DS(ON)}$ is recommended to be no lower than ~16.5/I_{OUT} (mΩ). For example, for a 5A application, the $R_{DS(ON)}$ of the MOSFET should be no lower than 3.3mΩ.

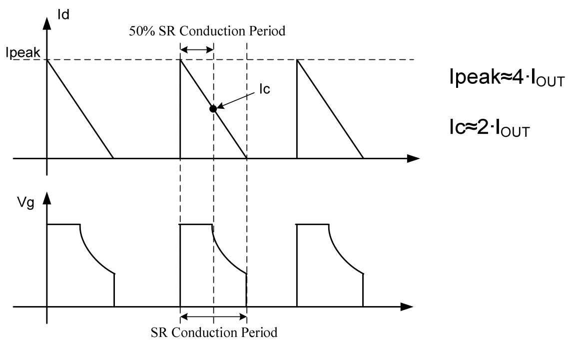
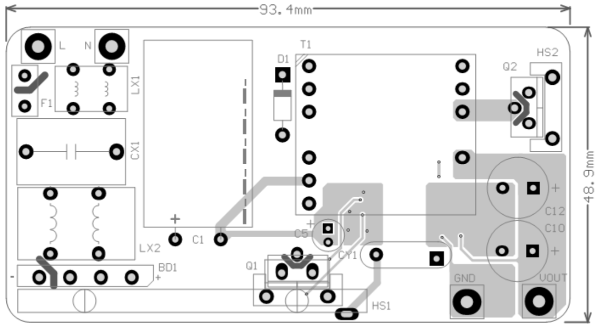


Figure 18: Synchronous Rectification Typical Waveforms in QR Flyback

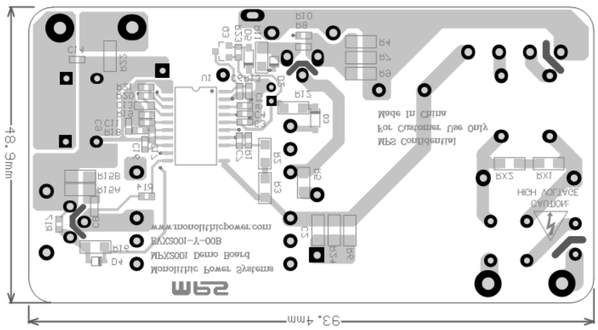
PCB Layout Guidelines

Efficient PCB layout is critical for reliable operation, good EMI performance, and good thermal performance. For best results, refer to Figure 19 and follow the guidelines below.

1) Minimize the power stage loop area.
   This includes the input loop (C1 - T1 - Q1 - R4/R7/R9 - C1), the auxiliary winding loop (T1 - D3 - R12 - C5 - T1), and the output loop (T1 - C10/C12 - Q2 - T1).
2) Separate the input loop GND and control circuit.
   They should only be connected at C1.
3) Connect the Q1 heat-sink to the primary GND plane to improve EMI.
4) Place the control circuit capacitors (such as those for FB, CS, COMP, and VCC) close to the IC to decouple noise.
5) Keep FB and COMP far from the noisy point.
   The coupled noise on FB or COMP can make the system unstable.
6) Place the sensing connection as close to the SR MOSFET as possible.
7) Make the sensing loop as small as possible and separate from the power loop.
8) Keep the IC output of the power loop to avoid the noise coupled on the IC.
9) Place the IC can underneath the transformer for tight design.
   If doing this, be sure to design the circuit carefully. Otherwise, COMP and FB can couple switching noise from the transformer.



Top



Bottom

Figure 19: 12V/5A Demo PCB Layout

Design Example

Table 1 is a design example of the MPX2001 for power adapter applications. The evaluation board name is EVX2001-Y-00C, which can be sampled. The related datasheet is available on the MPS website.

Table 1: 60W Design Example

V_{IN}	90 to 265V_{AC}
V_{OUT}	12V
I_{OUT}	5A

An evaluation kit is available for 45W USB PD design references.

TYPICAL APPLICATION CIRCUIT

Figure 20 shows a MPX2001 typical application circuit with universal input and 12V/5A output specification.

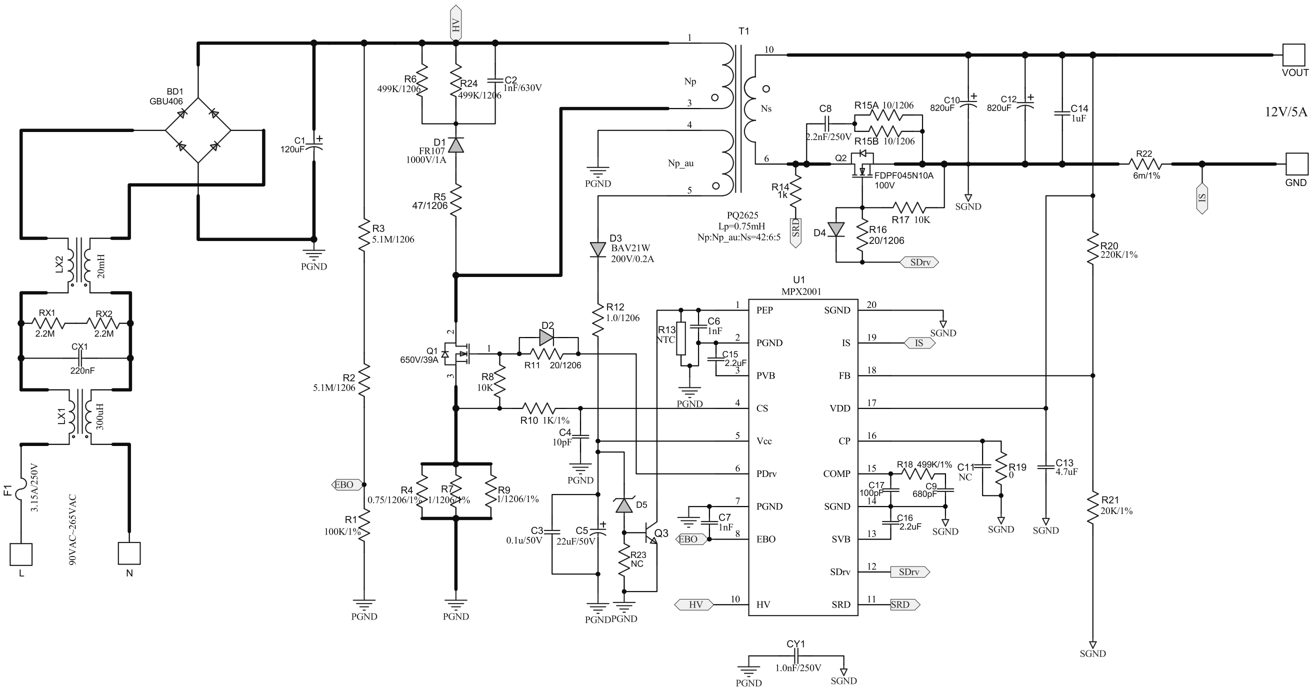
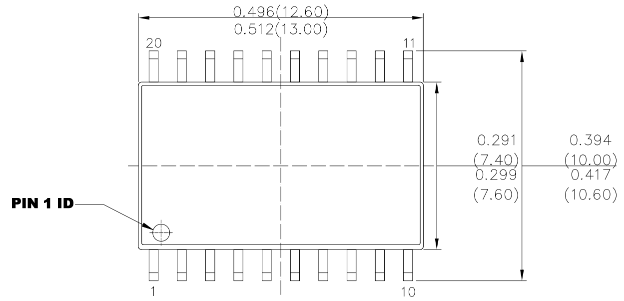


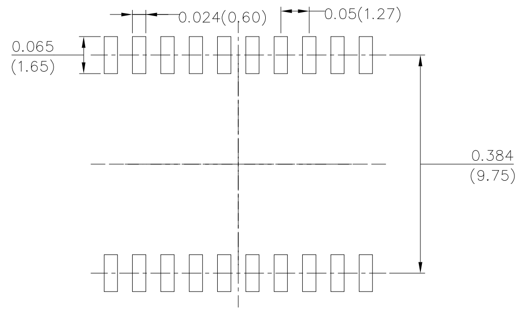
Figure 20: Example of a Typical Application

PACKAGE INFORMATION

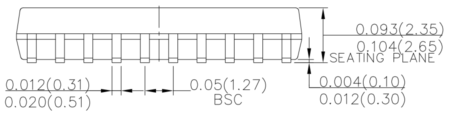
SOICW20



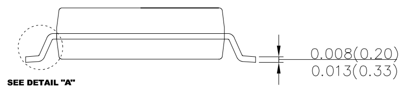
TOP VIEW



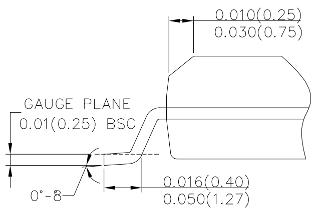
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



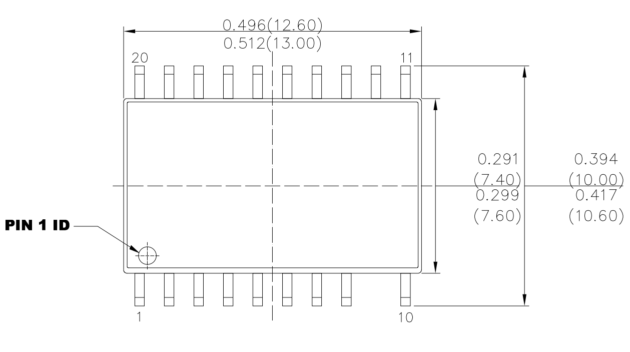
DETAIL "A"

NOTE:

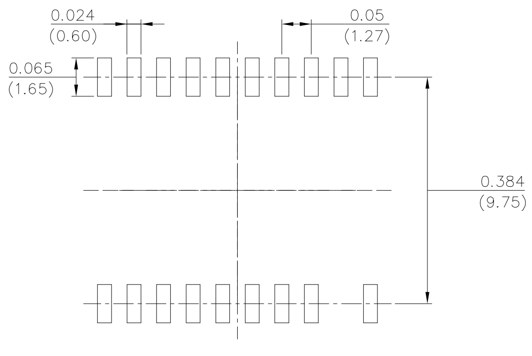
1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5) DRAWING REFERENCE TO JEDEC MS-013, VARIATION AC.
6) DRAWING IS NOT TO SCALE.

PACKAGE INFORMATION

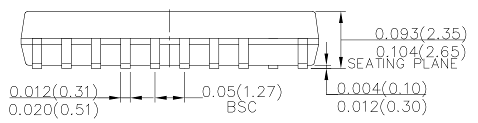
SOICW20-19



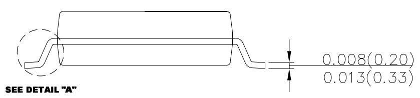
TOP VIEW



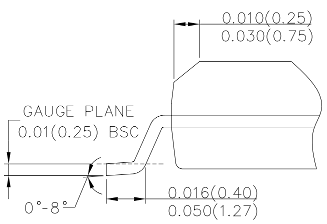
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



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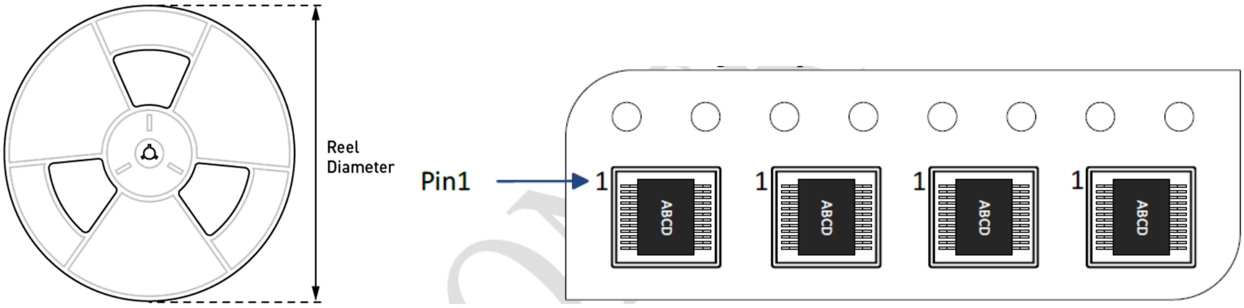
6) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity /Reel	Quantity /Tube	Quantity /Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch	Trailer Leader /Reel
MPX2001GY	SOICW20	1000	37	N/A	13in.	24mm	12mm	110&110
MPX2001GYE	SOICW20-19	1000	37	N/A	13in.	24mm	12mm	110&110