MagVector™ MV300

3D Magnetic Sensor with I²C and SPI Digital Output

DESCRIPTION

The MV300 is a magnetic sensor that detects the direction and strength of the 3D magnetic field (B_X, B_Y, and B_Z). The signal from the Hall sensors is amplified and converted to a digitized signal, and the magnetic field range is ±150mT.

The MV300 operates in host-controlled mode, auto sampling cycle (ASC) mode, or full-speed mode.

The MV300 features digital communication for readout and can be configured through either the I²C interface or serial peripheral interface (SPI).

The MV300 is available in a TSOT23-6 package.

FEATURES

- 3D (X, Y, and Z) Magnetic Sensing
- ±150mT Magnetic Field Range
- 12-Bit Data Length
- 0.2mT RMS Noise (X, Y) and 0.1mT RMS Noise (Z) at 20kHz Refresh Rate
- On-Chip Temperature Sensor
- 40µs Conversion Time per Channel
- Data Updates upon User Request in Host-Controlled Mode
- Selectable Update Rate in Auto Sampling Cycle (ASC) Mode
- I²C Interface or Serial Peripheral Interface (SPI) for Digital Readout and Chip Configuration
- 3.3V Supply, 2.5mA Current Consumption in Measuring State
- 30nA Current Consumption in Power-Down State
- -40°C to +125°C Operating Temperature Range
- Available in a TSOT23-6 Package

APPLICATIONS

- DC or AC Magnetic Field Detection
- Magnetic Field Mapping
- 3D Magnetic Joysticks
- Position Control

TYPICAL APPLICATIONS

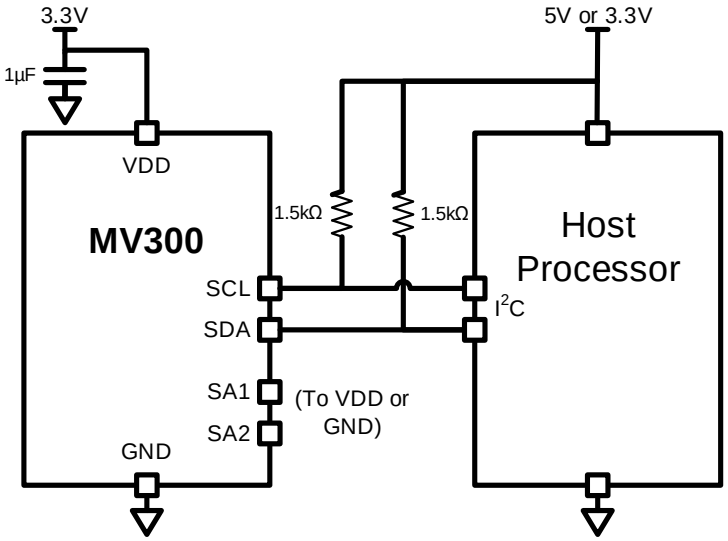


Figure 1: Typical Application (I^2C Version)

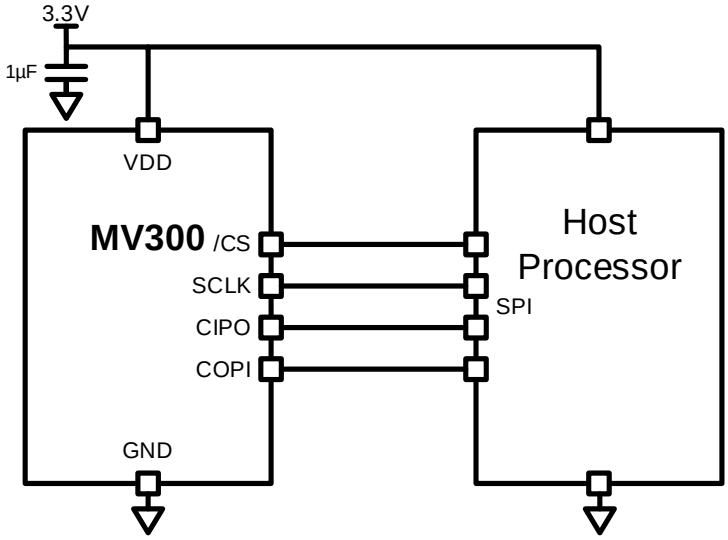


Figure 2: Typical Application (SPI Version)

ORDERING INFORMATION

Part Number	Package	Top Marking	MSL Rating	Communication
MV300GJ-C*	TSOT23-6	*See Below*	1	I^2C
MV300GJ-S*	TSOT23-6	*See Below*	1	SPI
TBMV300-Q-LT-I2C	Test board	N/A	N/A	I^2C
TBMV300-Q-LT-SPI	Test board	N/A	N/A	SPI
EVKT-MV-RP-PICO	Evaluation kit	N/A	N/A	N/A

* For Tape & Reel, add suffix -Z (e.g. MV300GJ-C-Z).

TOP MARKING

BVHY

BVH: Product code
Y: Year code

EVALUATION KIT (EVKT-MV-RP-PICO)

EVKT-MV-RP-PICO kit contents:

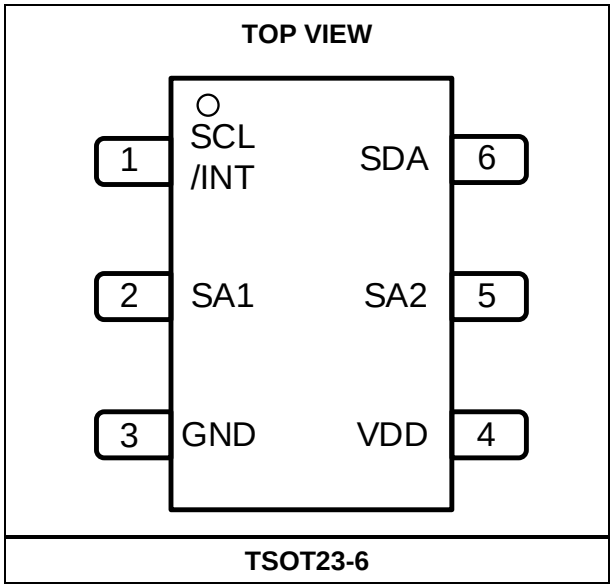
#	Part Number	Item	Quantity
1	EVKT-MV-RP-PICO	Microcontroller (MCU) board	1
2	Ribbon cable	Connects the EVKT-MV-RP-PICO-Q-00A to the TBMV300-Q-LT I^2C or SPI test board	1
3	USB cable	Connects the EVKT-MV-RP-PICO to the computer	1
4	MagVector™ evaluation app	Software that communicates with the EVKT-MV-RP-PICO. It can be downloaded from the MPS website	-

Order directly from MonolithicPower.com or our distributors.

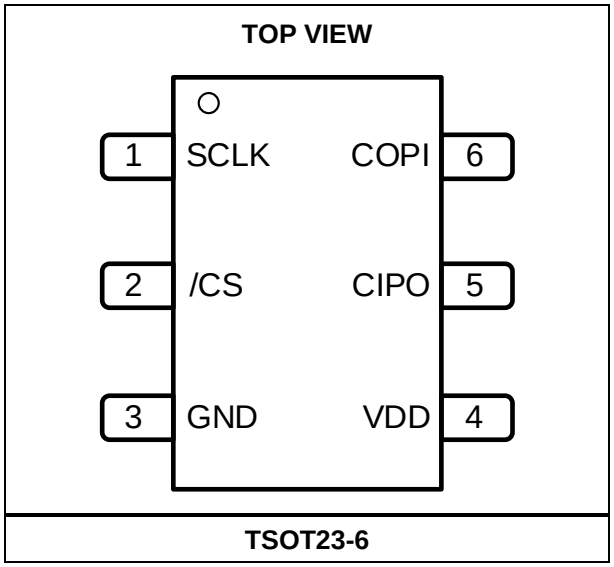
Figure 3: EVKT- MV-RP-PICO Evaluation Kit Set-Up

PACKAGE REFERENCE

I²C OUTPUT INTERFACE (MV300GJ-C)



SPI OUTPUT INTERFACE (MV300GJ-S)



PIN FUNCTIONS

I²C VERSION (MV300GJ-C)

Pin #	Name	Description
1	SCL, /INT	**Serial clock (I²C), interrupt.** The SCL, /INT pin is the input pin for I²C clock. It also indicates the data ready status. It is an open drain.
2	SA1	**I²C serial address definition.**
3	GND	**Supply ground.**
4	VDD	**3.3V supply.**
5	SA2	**I²C serial address definition.**
6	SDA	**Serial data (I²C).** The SDA pin is an open drain.

SPI VERSION (MV300GJ-S)

Pin #	Name	Description
1	SCLK	**Serial clock (SPI).**
2	/CS	**Chip select (SPI).**
3	GND	**Supply ground**
4	VDD	**3.3V supply**
5	CIPO	**Controller input peripheral output (SPI).** The CIPO pin is a push-pull pin when the SPI active; it is at a high impedance when the SPI is idle
6	COPI	**Controller output peripheral input (SPI).**

ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage (V_{DD}) .....-0.5V to +4.6V
Input pin voltage (V_{IN}) .....-0.5V to +4.6V
Output pin voltage (V_{OUT}) .....-0.5V to +4.6V
SCL, SDA pin voltage (V_{I2C}).....-0.5V to +6V
Continuous power dissipation (T_A = 25°C) (2)
..... 2W
Junction temperature (T_J) .....160°C
Lead temperature .....260°C
Storage temperature..... -65°C to +150°C

ESD Ratings

Human body model (HBM) ..... ±2kV
Charged-device model (CDM)..... ±1.5kV

Recommended Operating Conditions (3)

Supply voltage (V_{DD}) .....3V to 3.6V
Operating temperature..... -40°C to +125°C
Applied magnetic field..... 0mT to 150mT

Thermal Resistance (4) θ_{JA} θ_{JC}

TSOT23-6..... 143..... 76... °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can produce an excessive die temperature, and the regulator may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on a JESD51-7, 4-layer PCB.

GENERAL CHARACTERISTICS AT ROOM TEMPERATURE

V_{DD} = 3.3V, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Magnetic Characteristics						
Magnetic linear range	R_M			±150		mT
Sensitivity	S_M			7		LSB/mT
Offset (7)	$B_{O-X,Y}$	X and Y axes	-2.2		+2.2	mT
	B_{O-Z}	Z axis	-1.8		+1.8	mT
Noise RMS	$N_{X,Y-RMS}$	X and Y axes		0.2		mT
	N_{Z-RMS}	Z axis		0.1		mT
INL (8)	E_{INL}			±2		LSB
Magnetic matching	M_{X-Y} (5)			±1		%
	$M_{X,Y-Z}$ (6)			±10		%
Magnetic hysteresis	B_{HYS}			0		LSB

Notes:

5) The X to Y magnetic matching can be defined with Equation (1):

$$M_{X-Y} = 100 \times 2 \times \frac{S_X - S_Y}{S_X + S_Y} \quad (1)$$

6) The X/Y to Z magnetic matching can be defined with Equation (2):

$$M_{X,Y-Z} = 100 \times 2 \times \frac{S_X + S_Y - 2S_Z}{S_X + S_Y + 2S_Z} \quad (2)$$

GENERAL CHARACTERISTICS

V_{DD} = 3V to 3.6V, T_A = -40°C to +125°C, typical values at 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Supply voltage (7)	V_{DD}		3.0	3.3	3.6	V
Supply current	I_{PD}	Power-down state		30		nA
	I_{MEAS}	Measuring state (default measurement configuration)		2.5		mA
	I_{IDLE}	Idle state		70		µA
Accuracy						
Sensitivity drift X, Y, Z (7)	E_{SENSD}	Across the full temperature range and V_{DD} range	-17	±3	+17	%
Offset drift (7)	$B_{OD-X,Y}$	X and Y axes	-3.0		+3.0	mT
	B_{OD-Z}	Z axis	-0.7		+0.7	mT
Noise RMS (7)	$N_{X,Y-RMS}$	X and Y axes		0.2		mT
	N_{Z-RMS}	Z axis		0.1		mT
INL between -40°C to +125°C (8)	E_{INL}			±3		LSB
DNL between -40°C to +125°C	E_{DNL}			±2		LSB
Magnetic matching drift (7)	$M_{D-X,Y}$ (5)		-8.5	±4	+8.5	%
	$M_{D-X,Y\ Z}$ (6)		-8.5	±4	+8.5	%
Temperature Output						
Temperature output sensitivity	S_T			5		LSB/°C
Digital value at 25°C				330		LSB
Noise (RMS)	N_{T-RMS}			0.3		°C
Data Output						
Refresh rate	f_R	Single-channel, full-speed mode		20		kHz
Data output length	DL			12		bits
Response Time						
Power-up time	t_{PU}	V_{DD} > 2.9V		135		µs
Analog-to-digital converter (ADC) conversion time	t_{ADC}			40		µs
Period of time under host-controlled mode (7)	t_{HC}		200			µs
Digital I/O						
Input high voltage for SCL and SDA pins (7)	V_{IHI2C}		2.5		5.5	V
Input high voltage (7)	V_{IH}		2.5		3.6	V
Input low voltage	V_{IL}		-0.3		0.8	V
Output low voltage (7)	V_{OL}	I_{OL} = 4mA			0.4	V
Output high voltage (7)	V_{OH}	I_{OH} = 4mA	2.4			V
Rising edge slew rate	t_R	20% to 80 % of V_{DD}, C_L = 50pF		7		ns
Falling edge slew rate	t_F	20% to 80 % of V_{DD}, C_L = 50pF		7		ns

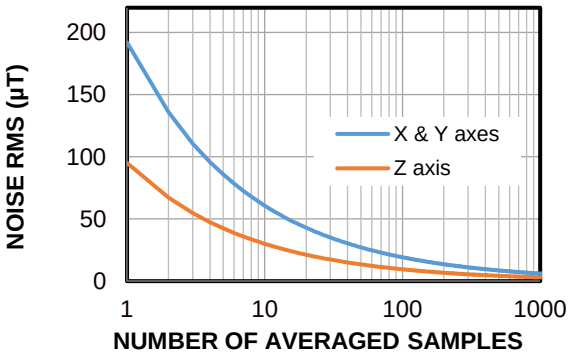
Notes:

7) Guaranteed by design or characterization.
8) Defined as the maximum difference between a best liner fit across the full range and the actual output. Expressed here in LSB.

TYPICAL CHARACTERISTICS

V_{DD} = 3.3V, T_A = 25°C, unless otherwise stated.

Noise RMS



FUNCTIONAL BLOCK DIAGRAM

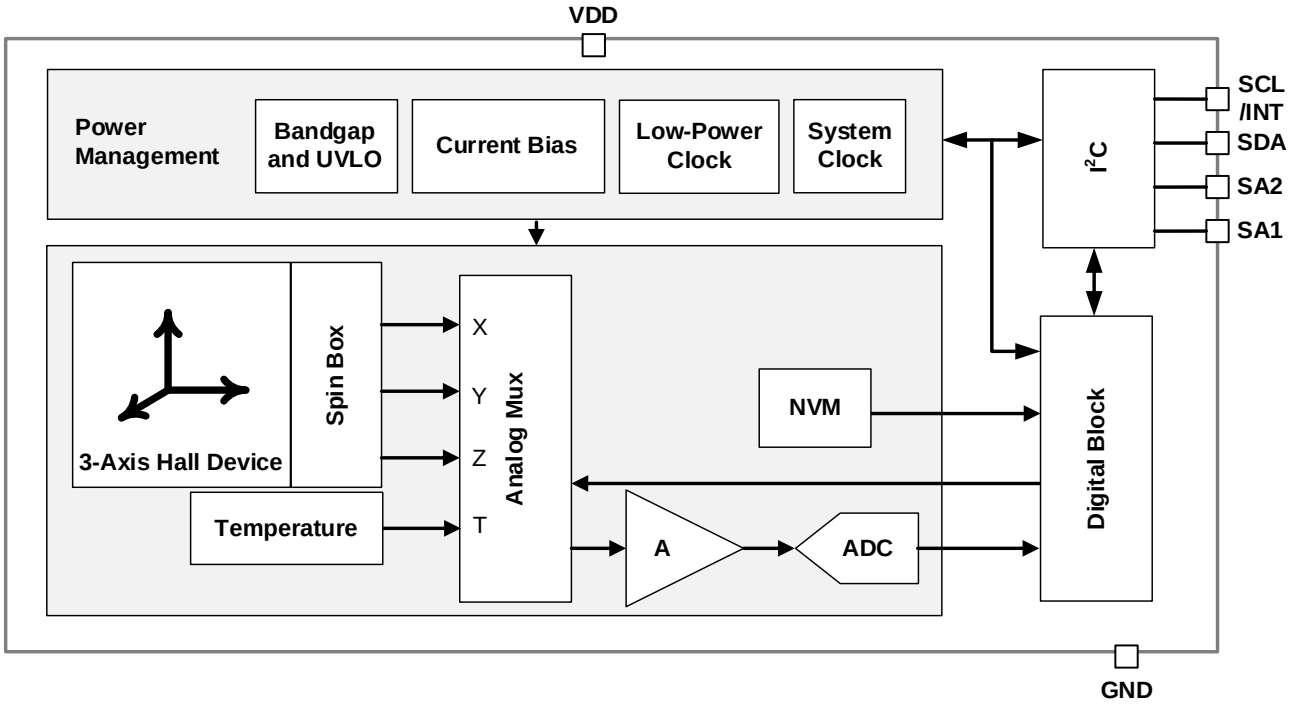


Figure 4: Functional Block Diagram (I²C Version)

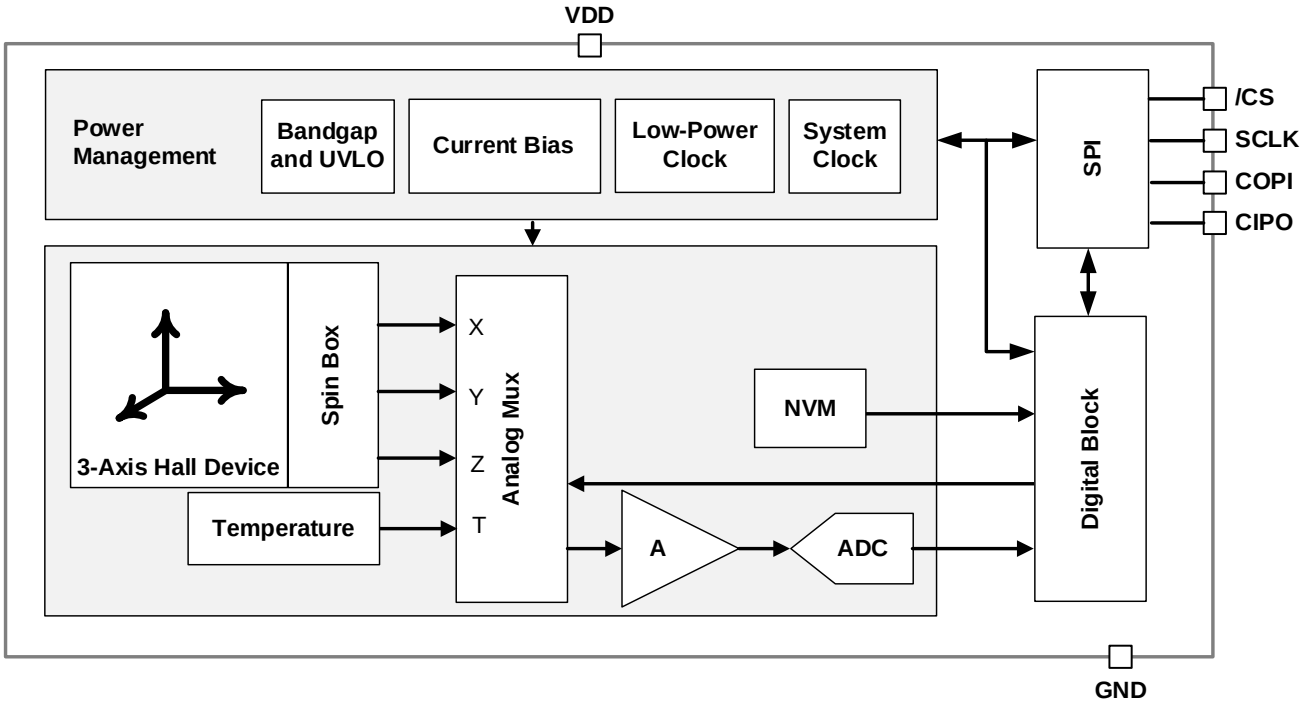


Figure 5: Functional Block Diagram (SPI Version)

OPERATION

Definition of Magnetic Field Direction

The MV300 senses 3D magnetic fields with integrated Hall devices. Figure 6 shows the positive direction of the detected magnetic field.

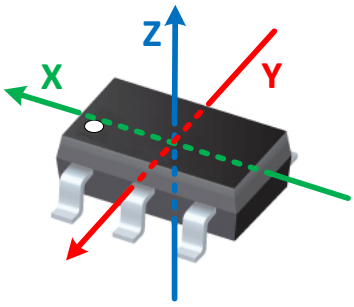


Figure 6: Definition of Magnetic Field Direction

Sensing Part Location

The MV300's sensitive area (where the Hall devices are placed) is confined within a 150µmx150µm square region. It is 0.5mm off-center in the X direction and 0.28mm above the package's bottom surface (see Figure 7).

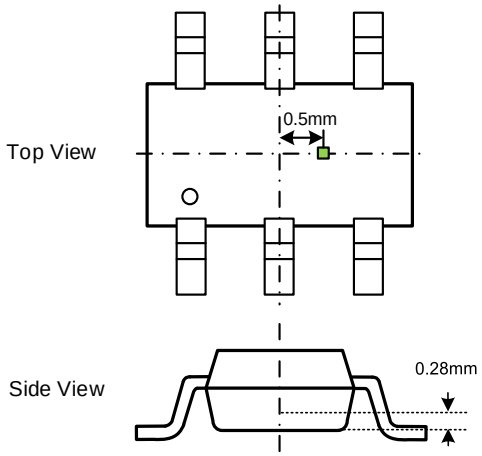


Figure 7: Sensing Part Location Inside the Package

Operating States

The sensor has three states of operation defining its power consumption: the power-down state, idle state, and measuring state.

Power-Down State

In this state, all blocks are off except for the digital block and I²C interface or serial peripheral interface (SPI) communication interface, providing ultra-low current consumption.

When the sensor is in the power-down state, the system clock follows one of the processes listed below:

- For the I²C version, when the sensor address is detected, the system clock turns on to enable communication.
- For the SPI version, when /CS is low, the system clock turns on to enable communication.

Idle State

In this state, only the digital block, communication interface, low-power clock, and bandgap run. The low-power clock turns on to support the automatic sampling rate.

When a communication request is detected, the system clock turns on to enable communication.

Measuring State

In this state, all blocks run, and the sensor performs the measurements.

Power Control Modes

By combining different operating states, the MV300 can operate in three different modes: host-controlled mode, auto sampling cycle (ASC) mode, or full-speed mode.

The operation mode is controlled by the MODE bits in the MODE1 (0x11) register.

Host-Controlled Mode

In this mode, the sensor mainly stays in the power-down state.

When the sensor receives the trigger command to perform a measurement, it goes into the measuring state. After the measurement is finished, the MV300 returns to the power-down state.

The average current in host-controlled mode can be calculated with Equation (3).

$$I_{HOST\text{-}CONTROLLED} = I_{MEAS} \times t_{MEAS} \times f_{UPDATE} \quad (3)$$

Where I_{MEAS} and t_{MEAS} are from Table 1 on page 12, and f_{UPDATE} is the update frequency, assuming that the host controller triggers the measurement periodically.

Auto Sampling Cycle (ASC) Mode

ASC mode alternates between the idle state and measuring state.

When the sensor is in the measuring state, it performs a single measurement on a pre-defined update rate, and returns to the idle state for the rest of the period.

The update rate of ASC mode is set by the UPDATERATE bits in the MODE2 (0x12) register.

The current consumption in ASC mode can be calculated with Equation (4):

$$I_{ASC} = I_{IDLE} \times \frac{t_{ASC} - t_{MEAS}}{t_{ASC}} + I_{MEAS} \times \frac{t_{MEAS}}{t_{ASC}} \quad (4)$$

Where t_{ASC} is the update period of the ASC mode, and I_{MEAS} and t_{MEAS} are shown in Table 1 on page 12.

Full-Speed Mode

In this mode, the MV300 always stays in the measuring state, continuously measuring the B_X, B_Y, B_Z, and T channels.

The current consumption in this mode is the measuring current, calculated with Equation (5):

$$I_{FULL\text{-}SPEED} = I_{MEAS} \quad (5)$$

I_{MEAS} is shown in Table 1 on page 12.

Measurement Sequence

Each measurement includes the 4 channels: B_X, B_Y, B_Z, and T.

The measurements are sequential and take 40µs per channel. The analog-to-digital converter (ADC) runs with the measurement, with a delay of 10µs. After the last channel is converted, all data is transferred to the registers.

In host-controlled mode, the host controller triggers the measurement sequence. There is a 5µs set-up delay between the trigger and the measurement of the first channel. For the I²C version, with the clock-stretching feature, the user can send a command frame before conversion ends (see Figure 8). For the SPI version, the user must wait until the conversion is completed; otherwise, the read-back value is from the previous conversion (see Figure 9).

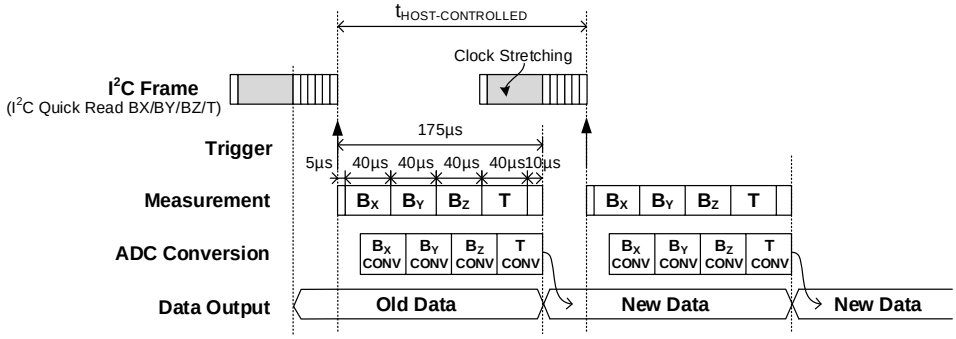


Figure 8: Measuring Sequence in Host-Controlled Mode for I²C Version (Trigger = 01)

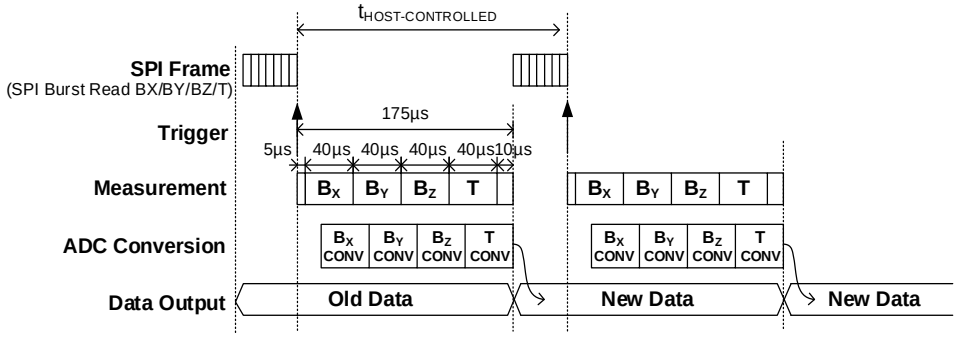


Figure 9: Measuring Sequence in Host-Controlled Mode for SPI Version (Trigger = 01)

In ASC mode, the measurement starts periodically. There is a 5µs set-up time delay before the first channel measurement (see Figure 10).

In host-controlled and ASC mode, it takes 175µs in total to perform one measurement for the B_X, B_Y, B_Z, and T channels. This time period goes from the set-up state to the register update.

In full-speed mode, the measurement works continuously, so there is no set-up time for each measurement (see Figure 11).

Table 1 shows a summary of measurement information.

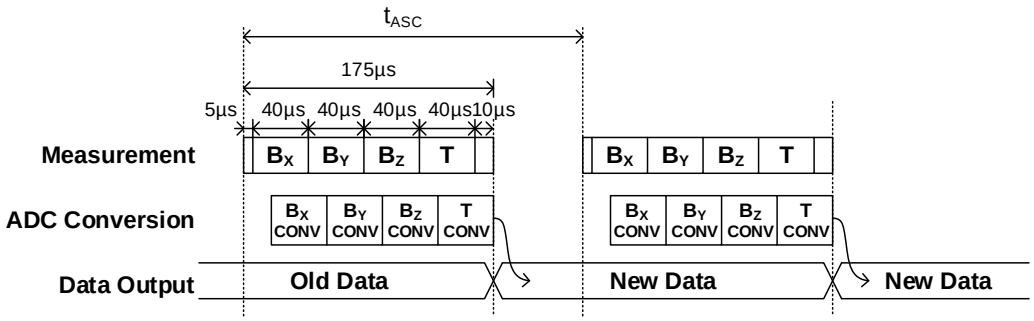


Figure 10: Measuring Sequence in ASC Mode

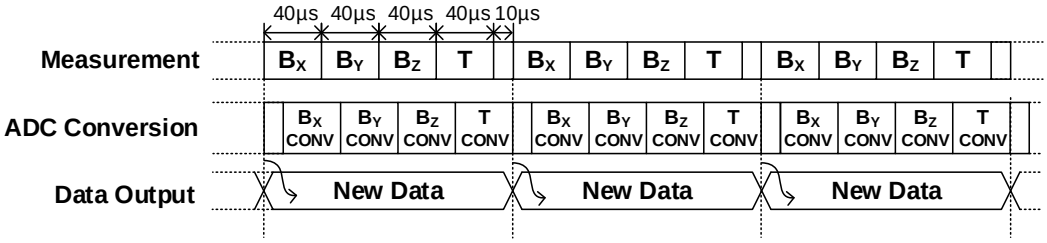


Figure 11: Measuring Sequence in Full-Speed Mode

Table 1: Summary of Measurement Information

Measurement Configuration	I_{MEAS} (mA)	t_{MEAS} (µs) in Full-Speed Mode	t_{MEAS} (µs) in Host-Controlled Mode and ASC Mode
B_X, B_Y, B_Z and T	2.5	170	175

Measurement Trigger

The measurement trigger determines the start of one measurement in host-controlled mode.

The trigger can be executed in two ways:

- For I²C quick read mode, the trigger is set by the TRIGMODE bits in the CONFIG (0x10) register.
- For other I²C communication modes and all SPI communication modes, the trigger is set by the 2-bit trigger in the command frame.

Table 2 shows the trigger setting and trigger mode.

Table 2: Trigger and Trigger Mode

2-Bit Trigger (TRIGMODE)	Trigger Mode
00	No measurement
01	Trigger measurement after write or read frame
10	Trigger measurement before the first MSB on the next byte

In ASC mode and full-speed mode, the trigger is ignored.

Interrupt and Wake-Up Operation

Interrupt and wake-up operation are only available in the MV300's I²C version, and these functions can only work in ASC mode.

Depending on the host microcontroller (MCU), the interrupt functionality might interfere with the correct operation of the I²C peripheral. One method to avoid this issue is to disable the MCU's I²C interface when waiting for an interrupt, and then enable it only immediately after the interrupt has been detected.

Interrupt

In ASC mode, a short pulse on the SCL, /INT line is generated every time an ADC conversion is completed, if the INTEN bit in the MODE1 (0x11) register is enabled.

This means that the SCL line is working as an interrupt, which indicates that ADC conversion is done. SCL is normally at the VDD voltage (V_{DD}). It is driven low when the interrupt occurs, and automatically recovers to V_{DD} after 1µs.

Threshold and Wake-Up Operation

If the interrupt is enabled, by enabling wake-up operation and setting the threshold, the SCL pin works as an interrupt, which is driven low only when the detected magnetic field exceeds the threshold boundary.

Wake-up operation is enabled by the WAKEUPEN bit in the THBXHILO0 (0x0D) register.

The user can set the upper and lower thresholds for each magnetic field component (B_X, B_Y, and B_Z) to monitor the magnetic field strength change or direction change. For example, the sensor measures magnetic field component B_X; if WAKEUPEN and INTEN both are enabled, the B_X value obtained from the measurement is compared to the threshold levels THBXHI, THBXLO, and an interrupt is generated if B_X exceeds THBXHI or is below THBXLO.

Table 3 shows the interrupt and wake-up operations. Figure 12 shows the interrupt behavior.

Table 3: Summary of Interrupt and Wake-Up Operation Under ASC Mode

INTEN	WAKEUPEN	Magnetic Field	MV300 Behavior
0	Any	Any	No interrupt sent on the SCL line
1	0	Any	Interrupt sent on the SCL line
1	1	Exceeds thresholds	Interrupt sent on the SCL line
1	1	Does not exceed the thresholds	No interrupt sent on the SCL line

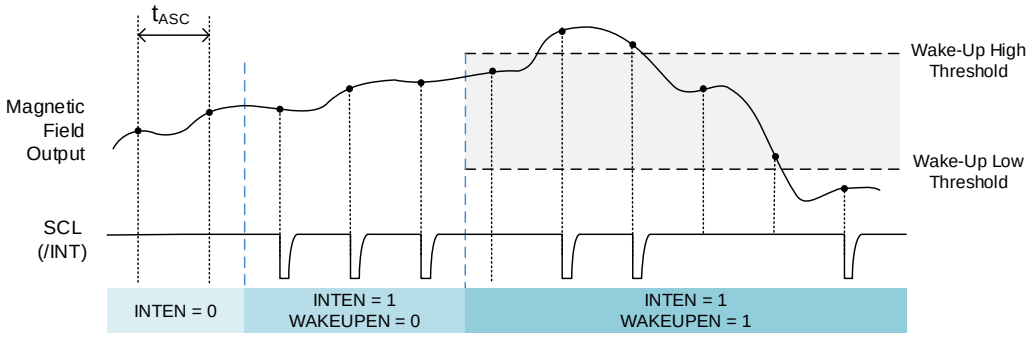


Figure 12: Example of Interrupt and Wake-Up Operation

I²C INTERFACE

The MV300's I²C implementation follows the I²C standard for bidirectional communication with a single controller. The sensor operates only as a peripheral device and is designed to operate in the fast-mode plus (FM+) I²C speed category (1Mbps).

The I²C protocol follows the mandatory features for peripheral devices defined by UM10204 (refer to the NXP I²C bus specification and user manual for more details). The device also supports clock stretching.

I²C Sensor Address Definition

By default, the 7-bit I²C sensor address (SA) is defined at start-up by the logic level of the SA2 and SA1 pins (see Table 4 on page 14).

After start-up, the sensor address does not change, even if the logic levels of the SA1 and SA2 pins change.

Table 4: SA Definition by the SA1/SA2 Pins

SA2	SA1	7-Bit SA (Hexadecimal)
0	0	0x14
0	1	0x15
1	0	0x16
1	1	0x17

Some applications might require an SA different than those that can be configured via the SA1/SA2 pins, such as when more than 4 MV300 devices are connected to the same I²C bus. In this scenario, it is possible to change the MV300's SA by configuring the SENSADDR (0x16) register:

- Set SENSADDR(0) = 1 to override the sensor address defined by SA1/SA2 at start-up.
- SENSADDR(7:1) should contain the target 7-bit sensor address value.

For example, to set the sensor address to 0x30, 0x61 should be written to the SENSADDR (0x16) register (see Table 5).

Table 5: SA Definition by SENSADDR

SENSADDR								SA
0	1	1	0	0	0	0	1	0x30
0	1	1	0	0	0	0	0	Power-up value

The SENSADDR (0x16) register is write-locked by default to prevent accidental modification. See the Register Unlock Sequence section on page 28 to unlock this register.

I²C Write Mode

Writing begins by sending the start condition, followed by the sensor address and write command (0). Then the user must send the 2-bit trigger and the register address (N(5:0)). The next byte contains the data to write (see Figure 13).

The user can write in a continuous manner by sending more bytes containing the data to be written. By doing so, the target register address is automatically incremented by one for each new data (see Figure 14).

To close the write mode sequence, the user must send a stop condition.

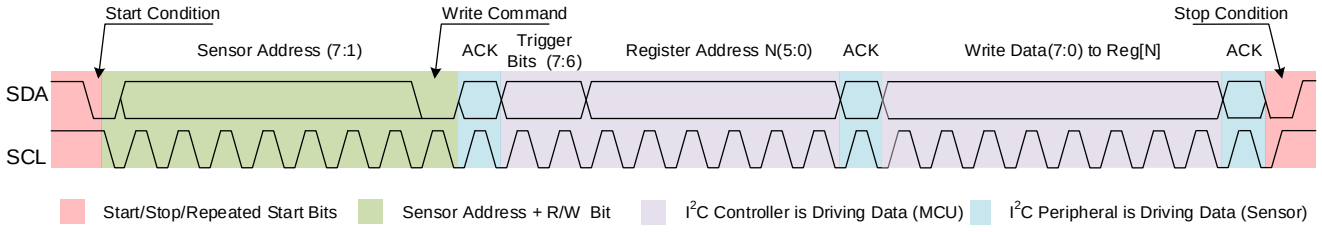


Figure 13: I²C Write Mode (Single Writing)

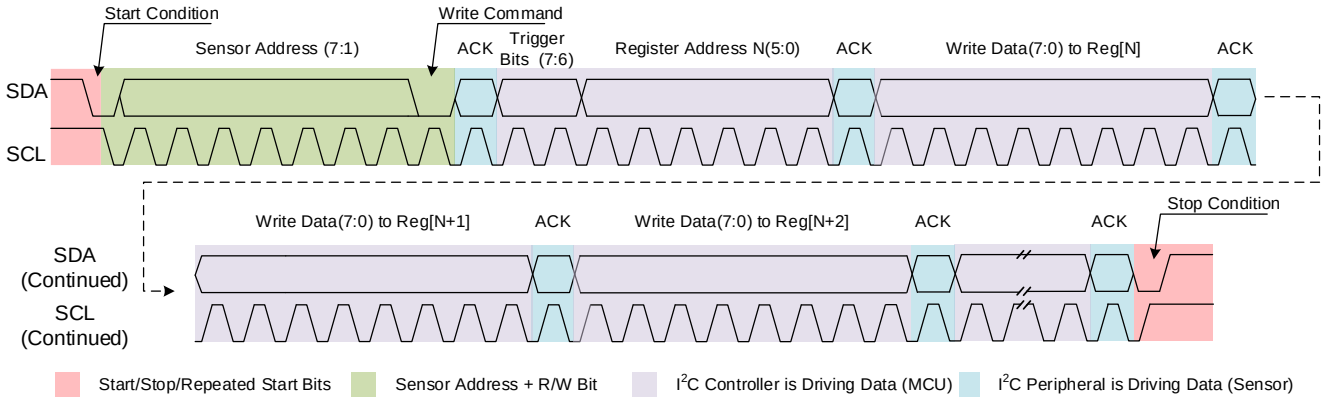


Figure 14: I²C Write Mode (Continuous Writing)

I²C Read Mode with Repeated Start

This mode allows a flexible read sequence at the expense of a larger data header, with a repeated start, sensor address, and the need to specify each target register address.

Communication starts by sending the start condition, then the controller sends the sensor address and write command (0) (see Figure 15). The next byte contains the 2-bit trigger and the address (*N*) of the register to be read, followed with a repeated start condition. The user must resend the MV300 address after the repeated start condition with a read command (1), and the MV300 responds with the register *N* value in the next byte.

A stop condtion must be sent to close communication.

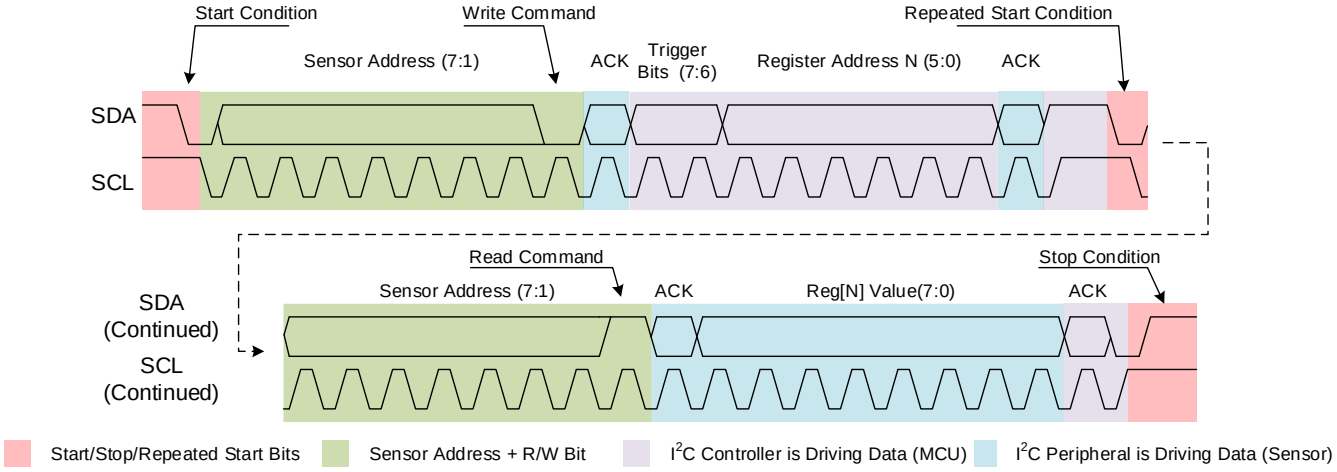


Figure 15: I²C Read Mode with Repeated Start

I²C Quick Read Mode

This mode provides a quick and easy way to read the sensor registers. It is recommended to use quick read mode to ensure that all the read data originate from the same measurement sequence.

In I²C quick read mode, the controller sends the start condition, sensor address, and the read command (1); the MV300 sequentially returns the data contained in registers 0x00~0x16 (see Figure 16). To close communication, a stop condition is required.

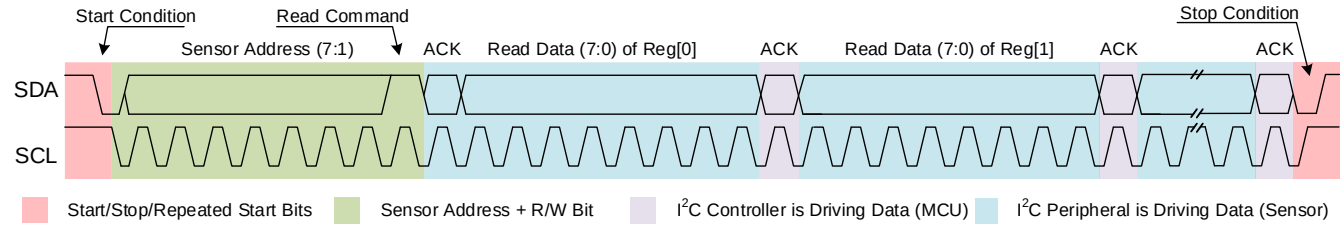


Figure 16: I²C Quick Read Mode

I²C Trigger

In host-controlled mode, the 2-bit trigger in the I²C command defines when the measurement is performed. Figure 17 on page 16 shows an example of a trigger event; when the trigger is 0b01, the measurement starts after the stop condition is received.

In I²C quick read mode, the trigger is controlled by TRIGMODE in the CONFIG (0x10) register (see Table 2 on page 12).

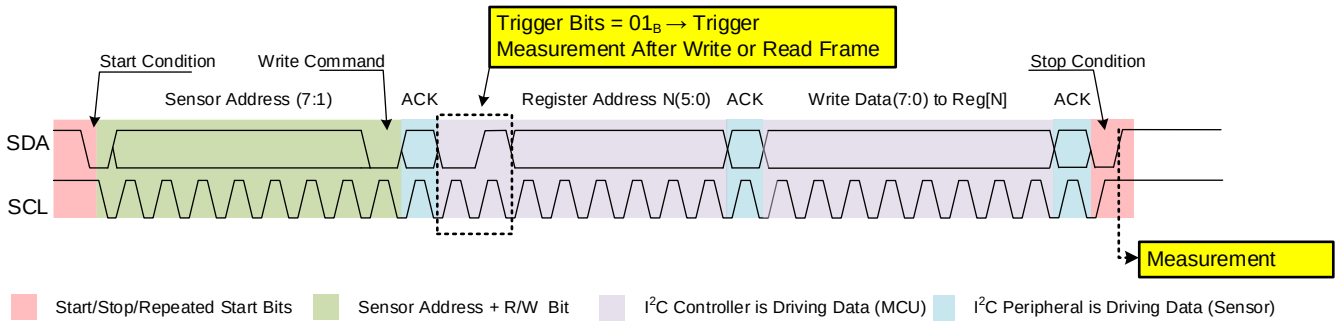


Figure 17: Example of I²C Trigger (Trigger Bits = 01_B)

I²C Clock Stretching

When the clock stretching function is used, the data is read after the ADC conversion is completed. This function helps to avoid reading old measurement results during an ADC conversion, which may occur when the ADC is updating the register while the host is reading it.

The clock stretching function is only applied to the read register command in quick read mode, and it does not affect the write command. Figure 18 shows an example of clock stretching applied to the quick read command.

Clock stretching can be applied to any power control mode, and it is enabled by default. Clock stretching pulls the SCL line low during the following situations:

- The ADC conversion is in progress.
- The sensor is about to transmit the valid acknowledge (ACK) in response to a read request from the I²C controller.

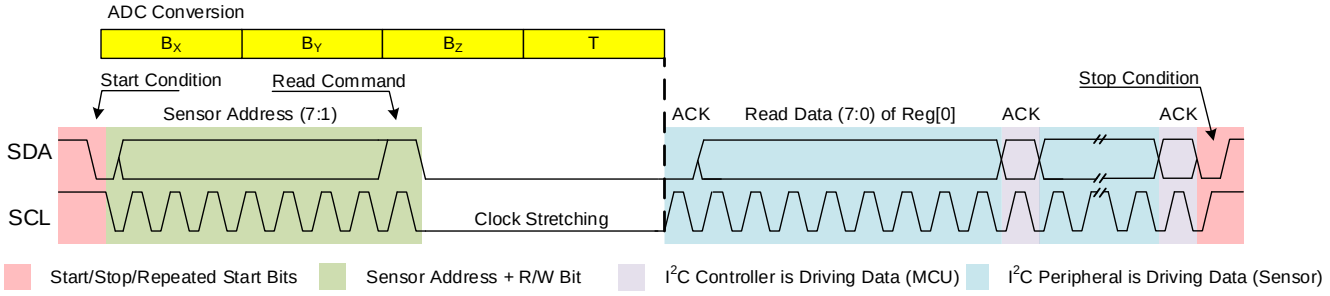


Figure 18: Clock Stretching Applied to Quick Read Mode

I²C Software Reset

The MV300 supports two I²C software reset commands, described below:

- NXP I²C specification software reset command: The user must send 0x00 and 0x06 on the SDA sequentially to execute a software reset. With a software reset, all registers return to the default values.
- MV300 software reset command: The user must perform three consecutive writes in the REGLOCKSEQ (0x14) register. The sequence of values to write is 0x52, 0x73, and 0x53.

SPI INTERFACE

The SPI is a four-wire, synchronous, serial communication interface. The MV300 supports SPI mode 0 and mode 3 (see Table 6 and Table 7 on page 17).

Table 6: SPI Specification

	Mode 0	Mode 3
SCLK Idle State	Low	High
Data Capture	On SCLK rising edge	
Data Transmission	On SCLK falling edge	
/CS Idle State	High	
Data Order	MSB first	

The SPI mode (0 or 3) is automatically detected by the sensor, so it does not require any action from the user.

Table 7: SPI Standard

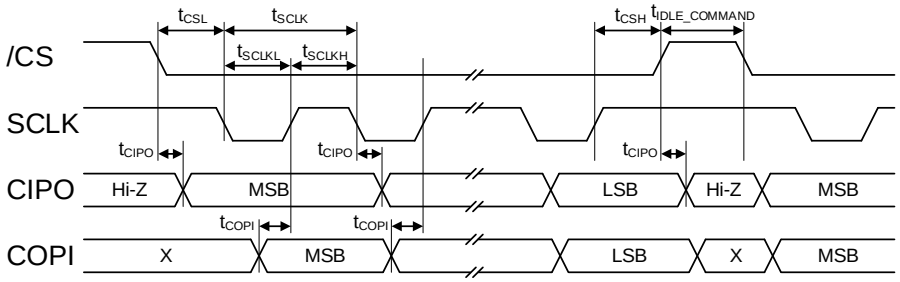
	Mode 0	Mode 3
CPOL	0	1
CPHA	0	1
Data Order (DORD)	0 (MSB first)	

The maximum SPI clock frequency is 1.2MHz, and there is no minimum clock frequency. The actual data rates depend on the PCB layout quality and signal trace length. Figure 19 and Table 8 show the SPI timing.

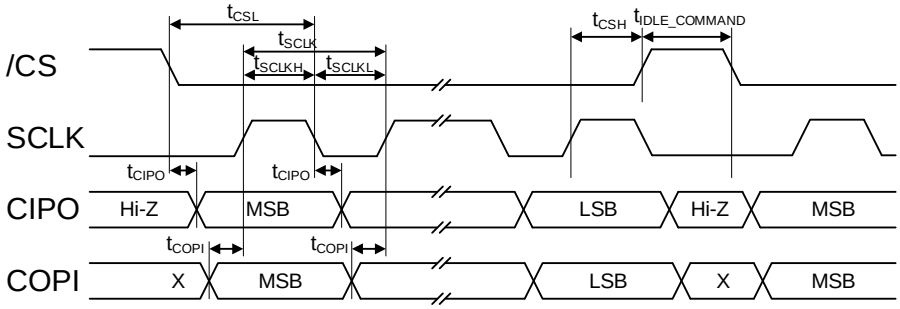
In this document, COPI stands for controller output peripheral input, while CIPO stands for controller input peripheral output.

All commands to the MV300 (whether for writing or reading a register content) must be transferred through the SPI COPI pin.

The MV300's SPI interface supports burst mode. The user should send multiple commands in sequence while /CS remains low. /CS must be set high after communication is completed; otherwise the MV300 always waits for communication.



SPI Mode 3



SPI Mode 0

Figure 19: SPI Timing Diagram

Table 8: SPI Timing

Parameter (9)	Description	Min	Max	Unit
$t_{IDLE\_COMMAND}$	Idle time between transmissions.	1		µs
t_{CSL}	Time between /CS falling edge and SCLK falling edge.	7		µs
t_{SCLK}	SCLK period.	1		µs
t_{SCLKL}	Duration of the low level of the SCLK signal.	500		ns
t_{SCLKH}	Duration of the high level of the SCLK signal.	500		ns
t_{CSH}	Time between SCLK rising edge and /CS rising edge.	2		µs
t_{CIPO}	SCLK setting edge to data output valid.	0	250	ns
t_{COPI}	Data input valid to SCLK reading edge.	417		ns

Note:

9) All values are guaranteed by design.

SPI communication is either:

- A read command
- A write command

The SPI communication frame is composed of a 2-bit trigger, the 1-bit R/W to define whether it is a read or write (respectively), and the 5-bit register address (see Table 9).

Table 9: SPI Communication Frame

	MSB							*LSB*
	7	*6*	*5*	*4*	*3*	*2*	*1*	*0*
COPI	**Trigger**		**R/W**	**Register Address**				

SPI Trigger

In host-controlled mode, the 2-bit trigger defines when the measurement is performed. In other power control modes, the trigger is ignored.

While /CS is low and several 8-bit commands are sent, the user should set the targeted trigger in the first byte, and then keep the trigger bit in the rest of the commands set to 00.

SPI Read Command

For reading, the first R/W must be set to 1. The register value is returned within the next communication frame (see Figure 20).

It is recommended to use SPI burst mode (e.g. maintain /CS as low as possible until all register values are read) to ensure that all the data were acquired in the same measurement period.

Figure 21 shows an example of an SPI burst mode reading.

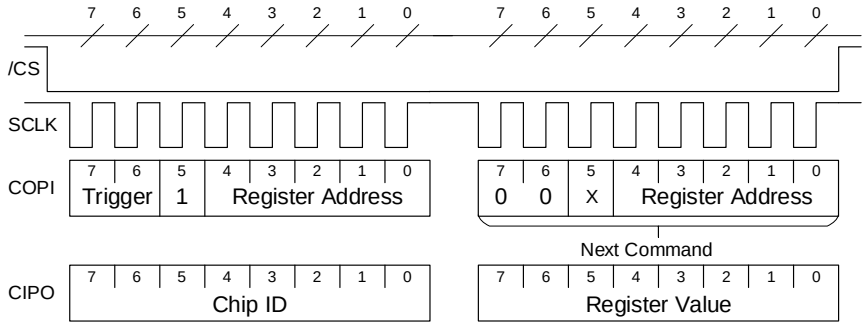


Figure 20: SPI Read Command

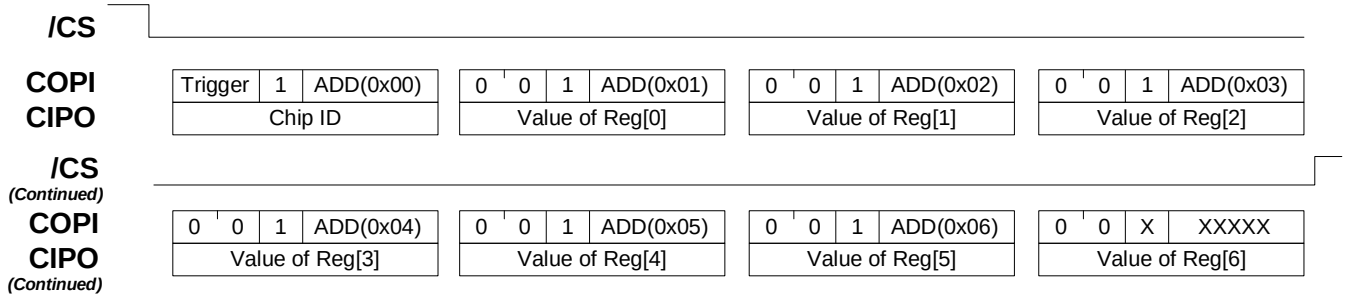


Figure 21: SPI Burst Mode Reading of a Complete Measurement

SPI Write Command

For writing, the first R/W must be set to 0. The register value to the write is sent within the next communication frame, and the written value is returned in the third communication frame (see Figure 22 on page 19). A 1µs delay should be added between the second frame and third frame to ensure that the read-back value is correct.

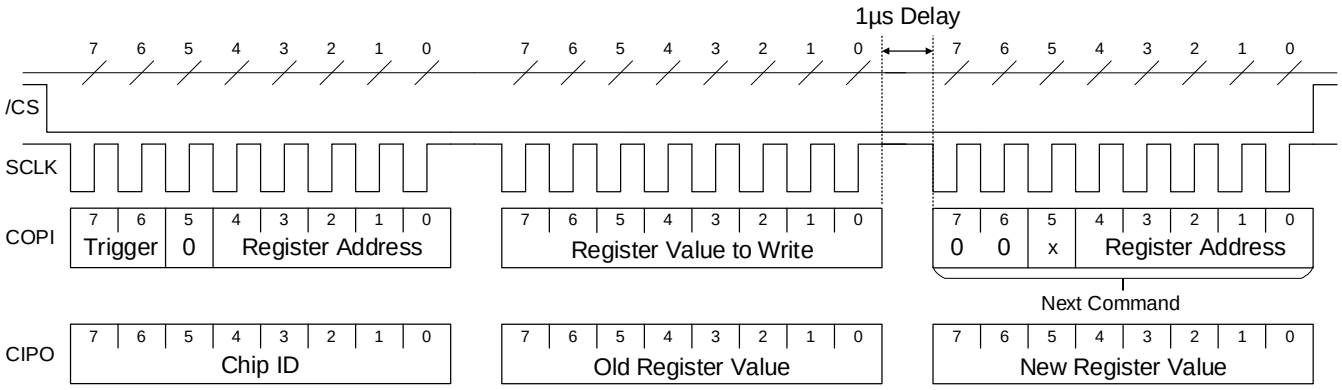


Figure 22: SPI Write Command

SPI Software Reset

A software reset can be performed via the SPI by sending a MV300 software reset command. See the I²C Software Reset section on page 16 for more information.

REGISTER MAP

Table 10: Register Map

Addr. (Hex)	Addr. (Dec)	Bit[7] MSB	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0] LSB
0x00	0	BX(11:4)							
0x01	1	BY(11:4)							
0x02	2	BZ(11:4)							
0x03	3	TEMP(11:4)							
0x04	4	BX(3:0)				BY(3:0)			
0x05	5	TEMP(3:2)		SENSID		BZ(3:0)			
0x06	6	RESERVED	CRCERROTP	TEMP(1:0)		RESERVED		FRMCNT	
0x07	7	THBXLO(11:4)							
0x08	8	THBXHI(11:4)							
0x09	9	THBYLO(11:4)							
0x0A	10	THBYHI(11:4)							
0x0B	11	THBZLO(11:4)							
0x0C	12	THBZHI(11:4)							
0x0D	13	RESERVED	WAKEUPEN	THBXHI(3:1)			THBXLO(3:1)		
0x0E	14	RESERVED		THBYHI(3:1)			THBYLO(3:1)		
0x0F	15	RESERVED		THBZHI(3:1)			THBZLO(3:1)		
0x10	16	RESERVED				TRIGMODE		RESERVED	
0x11	17	RESERVED					INTEN	MODE	
0x12	18	UPDATERATE			RESERVED				
0x13	19	DEVID							
0x14	20	REGLOCKSEQ							
0x16	22	SENSADDR							

REGISTER DESCRIPTION

BX1 (0x00)

The BX1 register contains the most significant bits (MSB) of the magnetic field value in the X direction (B_X).

Bits	Access	Bit Name	Default	Description
7:0	R	BX(11:4)	N/A	Bits[11:4] of B_X. See the Magnetic Field Value section on page 25 for additional information.

BY1 (0x01)

The BY1 register contains the MSB of the magnetic field value in the Y direction (B_Y).

Bits	Access	Bit Name	Default	Description
7:0	R	BY(11:4)	N/A	Bits[11:4] of B_Y. See the Magnetic Field Value section on page 25 for additional information.

BZ1 (0x02)

The BZ1 register contains the MSB of the magnetic field value in the Z direction (B_Z).

Bits	Access	Bit Name	Default	Description
7:0	R	BZ(11:4)	N/A	Bits[11:4] of B_Z. See the Magnetic Field Value section on page 25 for additional information.

TEMP1 (0x03)

The TEMP1 register contains the MSB of the temperature value.

Bits	Access	Bit Name	Default	Description
7:0	R	TEMP(11:4)	N/A	Bits[11:4] of TEMP. See the Temperature Value section on page 26 for additional information.

BXY0 (0x04)

The BXY0 register contains the least significant bits (LSB) of the magnetic field value in the X direction (B_X) and magnetic field value in the Y direction (B_Y).

Bits	Access	Bit Name	Default	Description
7:4	R	BX(3:0)	N/A	Bits[3:0] of B_X. See the Magnetic Field Value section on page 25 for additional information.
3:0	R	BY(3:0)	N/A	Bits[3:0] of B_Y. See the Magnetic Field Value section on page 25 for additional information.

TEMPBZ0 (0x05)

The TEMPBZ0 register contains the two bits of the temperature value, the I^2C sensor ID, and the LSB of the magnetic field value in the Z direction (B_Z).

Bits	Access	Bit Name	Default	Description
7:6	R	TEMP(3:2)	N/A	Bits[3:2] of the TEMP value. See the Temperature Value section on page 26 for additional information.
5:4	R	SENSID	N/A	Sets the I^2C sensor ID, which is the logic level of the SA2 and SA1 pins at start-up. SENSID[1]: SA2 pin logic level at start-up SENSID[0]: SA1 pin logic level at start-up
3:0	R	BZ(3:0)	N/A	Bits[3:0] of B_Z. See the Magnetic Field Value section on page 25 for additional information.

DIAG (0x06)

The DIAG register contains the one-time programmable (OTP) memory integrity check bit, the LSB of the temperature value, and the frame counter.

Bits	Access	Bit Name	Default	Description
7	N/A	RESERVED	N/A	Reserved.
6	R	CRCERROTP	N/A	Indicates if an OTP cyclic redundancy check (CRC) error was detected at start-up. See the OTP Integrity Check section on page 27 for additional information.
5:4	R	TEMP(1:0)	N/A	Bits[1:0] of the TEMP value. See the Temperature Value section on page 26 for additional information.
3:2	N/A	RESERVED	N/A	Reserved.
1:0	R	FRMCNT	N/A	Measurement frame counter. See the Frame Counter section on page 26 for additional information.

THBXLO1 (0x07)

The THBXLO1 register contains the most significant bits (MSB) of the low B_X threshold.

Bits	Access	Bit Name	Default	Description
7:0	R/W	THBXLO(11:4)	0x80	Bits[11:4] of the low B_X threshold. See the Wake-Up/Interrupt Setting and Threshold section on page 27 for additional information.

THBXHI1 (0x08)

The THBXHI1 register contains the MSB of the high B_X threshold.

Bits	Access	Bit Name	Default	Description
7:0	R/W	THBXHI(11:4)	0x7F	Bits[11:4] of the high B_X threshold. See the Wake-Up/Interrupt Setting and Threshold section on page 27 for additional information.

THBYLO1 (0x09)

The THBYLO1 register contains the MSB of the low B_Y threshold.

Bits	Access	Bit Name	Default	Description
7:0	R/W	THBYLO(11:4)	0x80	Bits[11:4] of the low B_Y threshold. See the Wake-Up/Interrupt Setting and Threshold section on page 27 for additional information.

THBYHI1 (0x0A)

The THBYHI1 register contains the MSB of the high B_Y threshold.

Bits	Access	Bit Name	Default	Description
7:0	R/W	THBYHI(11:4)	0x7F	Bits[11:4] of the high B_Y threshold. See the Wake-Up/Interrupt Setting and Threshold section on page 27 for additional information.

THBZLO1 (0x0B)

The THBZLO1 register contains the MSB of the low B_Z threshold.

Bits	Access	Bit Name	Default	Description
7:0	R/W	THBZLO(11:4)	0x80	Bits[11:4] of the low B_Z threshold. See the Wake-Up/Interrupt Setting and Threshold section on page 27 for additional information.

THBZHI1 (0x0C)

The THBZHI1 register contains the most significant bits (MSB) of the high B_Z threshold.

Bits	Access	Bit Name	Default	Description
7:0	R/W	THBZHI(11:4)	0x7F	Bits[11:4] of the B_Z high threshold. See the Wake-Up/Interrupt Setting and Threshold section on page 27 for additional information.

THBXHILO0 (0x0D)

The THBXHILO0 register contains the wake-up operation enable bit and the least significant bits (LSB) of the high and low B_X thresholds.

Bits	Access	Bit Name	Default	Description
7	N/A	RESERVED	0	Reserved. Do not change this value.
6	R/W	WAKEUPEN	0	Enables wake-up operation. See the Wake-Up/Interrupt Setting and Threshold section on page 27 for additional information.
5:3	R/W	THBXHI(3:1)	0b111	Bits[3:1] of the high B_X threshold. Bit[0] of the threshold cannot be configured, and it is always 0. See the Wake-Up/Interrupt Setting and Threshold section on page 27 for additional information.
2:0	R/W	THBXLO(3:1)	0b000	Bits[3:1] of the low B_X threshold. Bit[0] of the threshold cannot be configured, and it is always 0. See the Wake-Up/Interrupt Setting and Threshold section on page 27 for additional information.

THBYHILO0 (0x0E)

The THBYHILO0 register contains the LSB of the high and low B_Y thresholds.

Bits	Access	Bit Name	Default	Description
7:6	N/A	RESERVED	N/A	Reserved.
5:3	R/W	THBYHI(3:1)	0b111	Bits[3:1] of the high B_Y threshold. Bit[0] of the threshold cannot be configured, and it is always 0. See the Wake-Up/Interrupt Setting and Threshold section on page 27 for additional information.
2:0	R/W	THBYLO(3:1)	0b000	Bits[3:1] of the low B_Y threshold. Bit[0] of the threshold cannot be configured, and it is always 0. See the Wake-Up/Interrupt Setting and Threshold section on page 27 for additional information.

THBZHILO0 (0x0F)

The THBZHILO0 register contains the LSB of the high and low B_Z thresholds.

Bits	Access	Bit Name	Default	Description
7:6	N/A	RESERVED	0b00	Reserved. Do not change this value.
5:3	R/W	THBZHI(3:1)	0b111	Bits[3:1] of the high B_Z threshold. Bit[0] of the threshold cannot be configured, and it is always 0. See the Wake-Up/Interrupt Setting and Threshold section on page 27 for additional information.
2:0	R/W	THBZLO(3:1)	0b000	Bits[3:1] of the low B_Z threshold. Bit[0] of the threshold cannot be configured, and it is always 0. See the Wake-Up/Interrupt Setting and Threshold section on page 27 for additional information.

CONFIG (0x10)

The CONFIG register configures the measurement trigger.

Bits	Access	Bit Name	Default	Description
7:4	N/A	RESERVED	0b0000	Reserved. Do not change this value.
3:2	R/W	TRIGMODE	0b00	Trigger for I²C quick read mode. See the Measurement Trigger section on page 12 for additional information.
1:0	R	RESERVED	0b00	Reserved. Do not change this value.

MODE1 (0x11)

The CONFIG0 register enables the interrupt and configures the sensor operation mode.

Bits	Access	Bit Name	Default	Description
7:3	N/A	RESERVED	0b00000	Reserved. Do not change this value.
2	R/W	INTEN	0	Enables the interrupt. See the Interrupt section on page 13 for additional information.
1:0	R/W	MODE	0b00	Configures the sensor operation mode. See the Power Control Modes section on page 10 for additional information.

MODE2 (0x12)

The MODE2 register contains the bits to configure the ASC mode update rate.

Bits	Access	Bit Name	Default	Description
7:5	R/W	UPDATERATE	0b000	Sets the measurement update rate in ASC mode. See the Power Control Modes on page 10 for additional information.
4:0	N/A	RESERVED	0b00000	Reserved. Do not change this value.

DEVICEID (0x13)

The DEVICEID register contains the device ID.

Bits	Access	Bit Name	Default	Description
7:0	R	DEVID	0x30	Returns the MV300 device ID.

REGLOCKSEQ (0x14)

The REGLOCKSEQ register writes an unlock sequence to allow for write access to the SENSADDR register.

Bits	Access	Bit Name	Default	Description
7:0	R/W	REGLOCKSEQ	0x00	Writes the unlock sequence to unlock write access to the register SENSADDR. See the Register Unlock Sequence section on page 28 for additional information.

SENSADDR (0x16)

The SENSADDR register configures a custom I²C sensor address.

Bits	Access	Bit Name	Default	Description
7:0	R/W	SENSADDR	0x28	Overrides the I²C sensor address defined by the SA2 and SA1 pins level at start-up. See the I²C Sensor Address Definition section on page 13 for additional information.

REGISTER SETTINGS

Magnetic Field Value

The measurement values of the magnetic fields are represented as a 12-bit signed value (two's complement coding). Each magnetic field value is divided into an 8-bit MSB and a 4-bit LSB stored in the registers (see Table 11).

Table 11: Magnetic Field Component in Register

Magnetic Field Component	8-Bit MSB	Register Address of MSB	4-Bit LSB	Register Address of the LSB
B_X	BX(11:4)	BX1(7:0)	BX(3:0)	BXY0(7:4)
B_Y	BY(11:4)	BY1(7:0)	BY(3:0)	BXY0(3:0)
B_Z	BZ(11:4)	BZ1(7:0)	BZ(3:0)	TEMPBZ0(3:0)

Convert the sensor's digital output into a magnetic field unit with Equation (6):

$$B_{X,Y,Z}(mT) = \frac{B_{X,Y,Z}(11:0)}{S_M} \quad (6)$$

Typically, S_M = 7LSB/mT.

For example, if BX(11:4) = 0b1101 1011 and BX(3:0) = 0b0100, then BX = 0b1101 1011 0100 (see Table 12). When the MSB is 1, the corresponding decimal value is negative.

Table 12: Magnetic Conversion Table

	Bit[11] (MSB)	Bit[10]	Bit[9]	Bit[8]	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0] (LSB)
Decimal	-2048	1024	512	256	128	64	32	16	8	4	2	1
Binary	1	1	0	1	1	0	1	1	0	1	0	0

The signed decimal value of B_X can be calculated with Equation (7):

$$-2048 + 1024 + 256 + 128 + 32 + 16 + 4 = -588 \quad (7)$$

B_X (in mT) can be calculated with Equation (8):

$$B_X = -\frac{588}{7} = -84mT \quad (8)$$

Table 13 shows more examples of magnetic field conversion.

Table 13: Magnetic Field Conversion Example

12-Bit Binary	12-Bit Hexadecimal	Decimal (Signed)	Magnetic Field (mT)
0000 0000 0000	0x000	+0	0
0000 0000 0001	0x001	+1	+0.142
0111 1111 1111	0x7FF	+2047	+292.428
1000 0000 0000	0x800	-2048	-292.571
1000 0000 0001	0x801	-2047	-292.428
1101 1011 0100	0xDB4	-588	-84.000
1111 1111 1110	0xFFE	-2	-0.285
1111 1111 1111	0xFFF	-1	-0.142

Temperature Value

The temperature is a 12-bit signed value (two's complement coding), which is split into 3 different register addresses:

- TEMP(11:4) = TEMP1(7:0)
- TEMP(3:2) = TEMPBZ0(7:6)
- TEMP(1:0) = DIAG(5:4)

The converted temperature (in °C) can be calculated with Equation (9):

$$T(°C) = \frac{TEMP(11:0)}{S_T} - 41°C \quad (9)$$

Where S_T is typically 5LSB/°C.

For example, if TEMP(11:4) = 0b0001 0100, TEMP(3:2) = 0b10, and TEMP(1:0) = 0b10, then TEMP = 0b0001 0100 1010 (see Table 14). When the MSB is 1, the corresponding decimal value is negative.

Table 14: Temperature Conversion Table

	Bit[11] (MSB)	Bit[10]	Bit[9]	Bit[8]	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0] (LSB)
Decimal	-2048	1024	512	256	128	64	32	16	8	4	2	1
Binary	0	0	0	1	0	1	0	0	1	0	1	0

The signed decimal value of TEMP can be calculated with Equation (10):

$$256 + 64 + 8 + 2 = 330 \quad (10)$$

The temperature (in °C) can be calculated with Equation (11):

$$T = \frac{330}{5} - 41 = 25°C \quad (11)$$

Table 15 shows more examples of the temperature calculation.

Table 15: Temperature Value Conversion Example

TEMP(11:4)	TEMP(3:2)	TEMP(1:0)	TEMP(11:0)	Decimal (Signed)	Temperature (°C)
0000 0000	00	00	0000 0000 0000	0	-41
0000 1100	11	01	0000 1100 1101	205	0
0001 0100	10	10	0001 0100 1010	330	+25
0010 1100	00	01	0010 1100 0001	705	+100

Frame Counter

The frame counter (FRMCNT) in the DIAG (0x06) register is a 2-bit value that is automatically incremented by the sensor when a new measurement is completed.

This value can be checked to verify that the latest read value is from a new measurement. An identical FRMCNT value for two successive measurements indicates that the same measurement was read twice.

Power Control Modes

The MV300 has three modes to control the power (see the Power Control Modes section on page 10 for more details). The power control mode is controlled by a 2-bit parameter (MODE) in the MODE1 (0x11) register (see Table 16).

Table 16: Operation Mode

MODE	Mode
00	ASC Mode
01	Host-Controlled Mode
10	Full-Speed Mode
11	

In ASC mode, the update rate is determined by the 3-bit parameter (UPDATERATE) in the MODE2 (0x12) register. Table 17 shows different update rate settings in ASC mode.

Table 17: Update Rate in ASC Mode

Update Rate	Update Rate (Hz)	Update Period (t_{ASC}) (ms)
000 (default)	770	1.29
001	97	10.31
010	24	41.67
011	12	83.33
100	6	166.67
101	3	333.33
110	0.4	2500
111	0.05	20000

OTP Integrity Check

At start-up, the sensor restores the factory calibration parameters from the OTP memory. During this operation, the sensor computes the CRC value of the restored registers and compares it to the checksum stored in the OTP. If these values do not match, CRCERROTP in DIAG (0x06) register is set to 1. This error indicates that the factory calibration was not restored correctly.

Wake-Up/Interrupt Setting and Threshold

Wake-up operation must be used together with the interrupt. It is only available in the I^2C version under ASC mode (see the Interrupt and Wake-Up Operation section on page 12 for more details).

Wake-up operation is enabled when WAKEUPEN in the THBXHILO (0x0D) register is set to 1. The interrupt is enabled when INTEN in the MODE1 (0x11) register is set to 1.

The magnetic field wake-up threshold is a 12-bit signed value (two's complement coding). Each threshold is divided into an 8-bit MSB and 3-bit LSB, which can be configured in registers 0x07~0x0F. Bit[0] of each threshold is always 0 (see Table 18).

Table 18: Magnetic Field Threshold Value in Register

Threshold	8-Bit MSB	Register Address of MSB	3-Bit LSB	Register Address of LSB
B_X low threshold (THBXLO)	THBXLO(11:4)	THBXLO1(7:0)	THBXLO(3:1)	THBXHILO0(2:0)
B_X high threshold (THBXHI)	THBXHI(11:4)	THBXHI1(7:0)	THBXHI(3:1)	THBXHILO0(5:3)
B_Y low threshold (THBYLO)	THBYLO(11:4)	THBYLO1(7:0)	THBYLO(3:1)	THBYHILO0(2:0)
B_Y high threshold (THBYHI)	THBYHI(11:4)	THBYHI1(7:0)	THBYHI(3:1)	THBYHILO0(5:3)
B_Z low threshold (THBZLO)	THBZLO(11:4)	THBZLO1(7:0)	THBZLO(3:1)	THBYHILO0(2:0)
B_Z high threshold (THBZHI)	THBZHI(11:4)	THBZHI1(7:0)	THBZHI(3:1)	THBYHILO0(5:3)

The threshold coding is same as the magnetic field coding (see Equation (6) on page 25).

For example, if THBX(11:4) = 0b1010 1110 and THBXLO(3:1) = 0b001, then THBXLO = 0b1010 1110 0010, see Table 19 for the conversion table.

Table 19: Threshold Conversion Table

	Bit[11] (MSB)	Bit[10]	Bit[9]	Bit[8]	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0] (LSB)
Decimal	-2048	1024	512	256	128	64	32	16	8	4	2	1
Binary	1	0	1	0	1	1	1	0	0	0	1	0 (always)

The signed decimal value of THBXLO can be calculated with Equation (12):

$$-2048 + 512 + 128 + 64 + 32 + 2 = -1310 \quad (12)$$

The low threshold of the B_X field can be calculated with Equation (13):

$$B_X = -\frac{1310}{7} = -187.14\text{mT} \quad (13)$$

Table 13 on page 25 shows a threshold conversion example.

Register Unlock Sequence

The I²C sensor address can be configured via the SENSADDR (0x16) register (see the I²C Sensor Address Definition section on page 13 for more details). By default, this register is write-locked to prevent accidental modification, which could compromise communication between the sensor and controller.

To unlock write access to the SENSADDR (0x16) register, the user should perform three consecutive single writes to the REGLOCKSEQ (0x14) register. The sequence of values to write is 0x9C, 0x47, and 0x3B. The SENSADDR (0x16) register can be write-locked again by writing 0x00 to the REGLOCKSEQ (0x14) register. Table 20 shows the sequence of write operations required to set the I²C sensor address to 0x30.

Table 20: Write Sequence to Set Sensor Address to 0x30

Step	Address (Decimal)	Value (Hexadecimal)	Comment
1	20	0x9C	First write of the unlock sequence.
2	20	0x47	Second write of the unlock sequence.
3	20	0x3B	Third write of the unlock sequence. Register SENSADDR is unlocked.
4	22	0x61	Set the sensor address to 0x30 (see the I²C Sensor Address Definition section on page 13 for more details).
5	20	0x00	Lock register SENSADDR.

APPLICATION INFORMATION

Supply Decoupling

It is recommended to place a 1µF decoupling capacitor on the VDD pin and close to the sensor, with a low-impedance path on the GND pin (see C1 in Figure 24 and Figure 25 on page 30).

In case of a noisy supply, an additional 100nF decoupling capacitor can be added (see C2 on Figure 24 and Figure 25 on page 30). This capacitor should be placed between the sensor and the 1µF capacitor.

To further improve the supply noise filtering, a ferrite bead (e.g. 60Ω at 100MHz) can be added on the VDD line (see FB1 in Figure 24 and Figure 25 on page 30).

Selecting the I²C Pull-Up Resistor

The I²C clock and data lines (SCL and SDA) are open drain. Pull-up resistors are required on these two lines. The resistors affect the rising edge slew rate of the signals. It is recommended to use 1.5kΩ resistors to guarantee the I²C's correct operation at all supported frequencies (see R1 and R2 in Figure 24 on page 30).

SPI Signals Routing on the PCB

Typically, a direct connection between the sensor and controller's SPI pins is sufficient to ensure a proper data transfer across the SPI bus. However, in specific situations (e.g. long signal traces or external EMI presence), it is possible to improve signal integrity by making special considerations during the PCB design — in particular for the SCLK line. The guidelines are detailed below:

- Properly shield all SPI signals with a GND plane on both sides of each trace, and place a GND plane underneath the SPI signals.
- Place vias along these traces to connect the top and bottom GND planes.
- To avoid EMI issues, route the SCLK signal away from the other SPI signals and noise sources. The distance should be at least three times the SCLK trace width.
- Insert an RC low-pass filter on SCLK (see Figure 12 on page 13). This RC filter must be located close to the sensor. It is recommended to use a 200Ω series resistor with a 10pF shunt capacitor to obtain a 80MHz filter cutting frequency.
- Use a star topology for the GND connection, and keep it as direct and short as possible to avoid ground loops.
- Insert RC low-pass filters on the CIPO and COPI signals (see Figure 23). The RC filter on COPI must be located close to the controller, while the filter on CIPO must be located close to the sensor. It is recommended to use a 200Ω resistor with a 10pF capacitor.
- Avoid a significant trace length mismatch between the SPI signals, especially between the CIPO, COPI, and SCLK signals. These signals should have similar propagation delays.
- If possible, avoid placing vias on the SCLK signal.

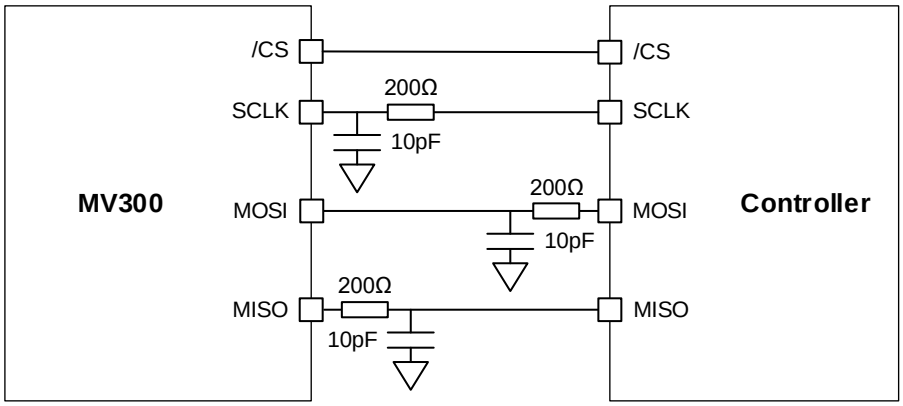


Figure 23: Examples of RC Low-Pass Filters on the SPI Signals

TYPICAL APPLICATION CIRCUITS

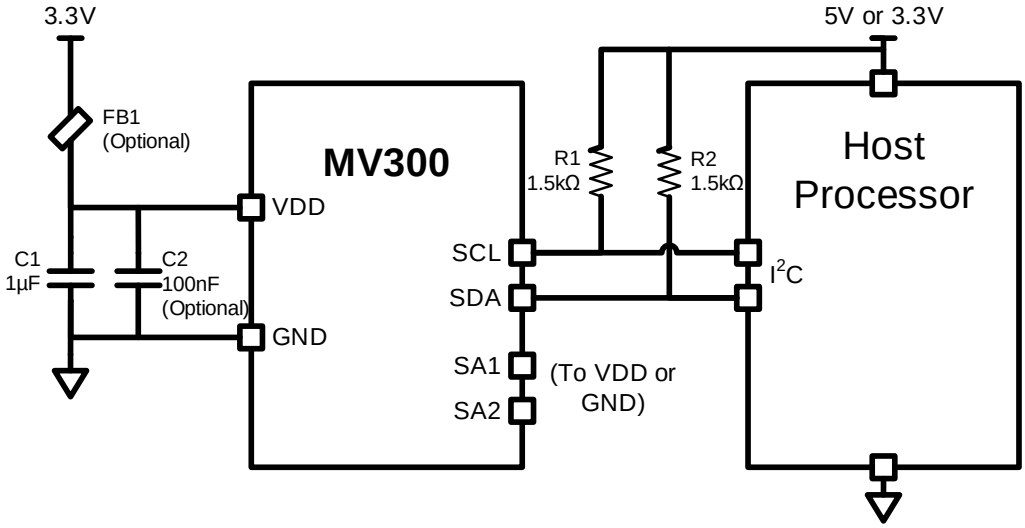


Figure 24: Typical Application Circuit (I^2C Version)

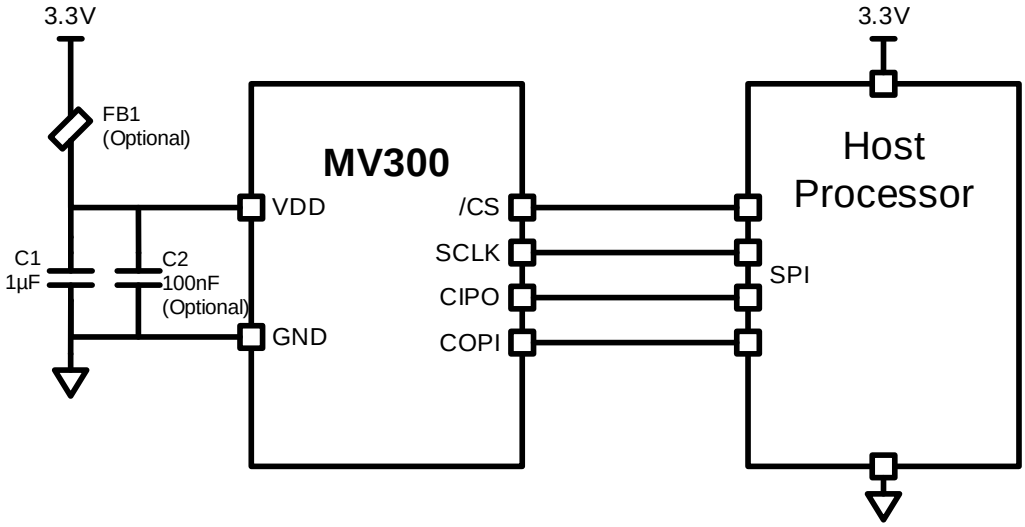
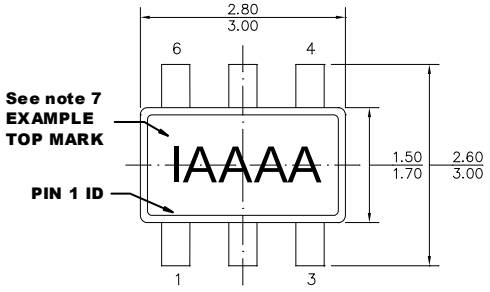


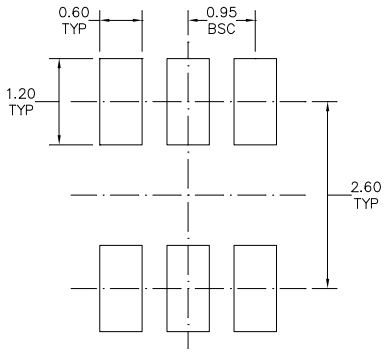
Figure 25: Typical Application Circuit (SPI Version)

PACKAGE INFORMATION

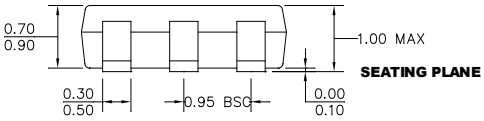
TSOT23-6



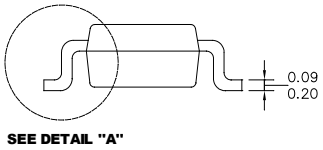
TOP VIEW



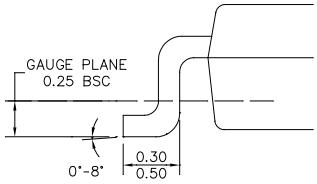
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW

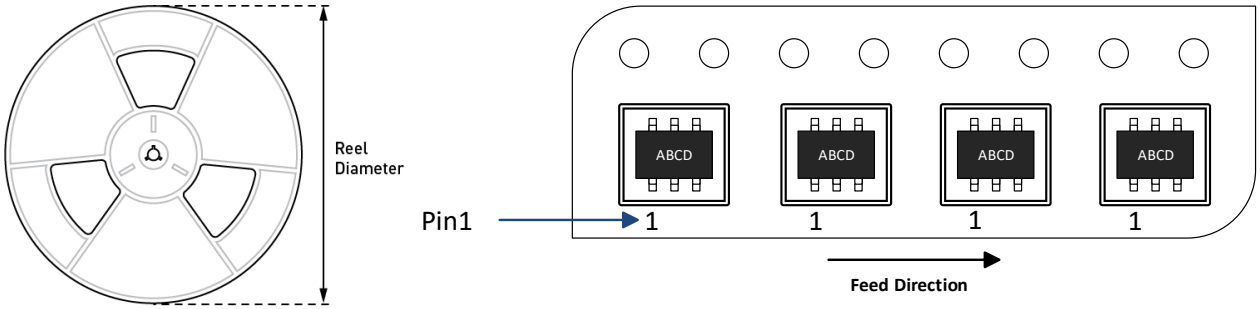


DETAIL "A"

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
5) DRAWING CONFORMS TO JEDEC MO-193, VARIATION AB.
6) DRAWING IS NOT TO SCALE.
7) PIN 1 IS LOWER LEFT PIN WHEN READING TOP MARK FROM LEFT TO RIGHT, (SEE EXAMPLE TOP MARK)

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MV300GJ-C-Z	TSOT23-6	3000	N/A	N/A	7in	8mm	4mm
MV300GJ-S-Z							

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	8/15/2024	Initial Release	-