mEZD81260A

16V/60A DC/DC Open Frame Module with Integrated Inductor

The Future of Analog IC Technology

END OF LIFE, REFER TO MPM3690-50B

DESCRIPTION

The mEZD81260A is a digital synchronous, step-down, COT control mode, open frame power module for high density DC/DC power application. It can provide 60A continuous output current.

The mEZD81260A is targeted for applications such as telecom and networking systems. It adopts digital control algorithm and can achieve fast transient response. It can be configured as dual phase or dual rail operation.

At the dual phase operation mode, the mEZD81260A has perfect interleaving and current sharing performance with proprietary digital technology used.

At the dual rail operation mode, the mEZD81260A can achieve programmable power on/off sequence.

The mEZD81260A need least external discrete components for sense and control circuit.

Almost all operation parameters and configuration parameters can be easily defined through PMBus commands with MPS digital programmable GUI.

The mEZD81260A provides full programmable fault protection features including: UVLO, UVP, OVP, OCP and OTP.

FEATURES

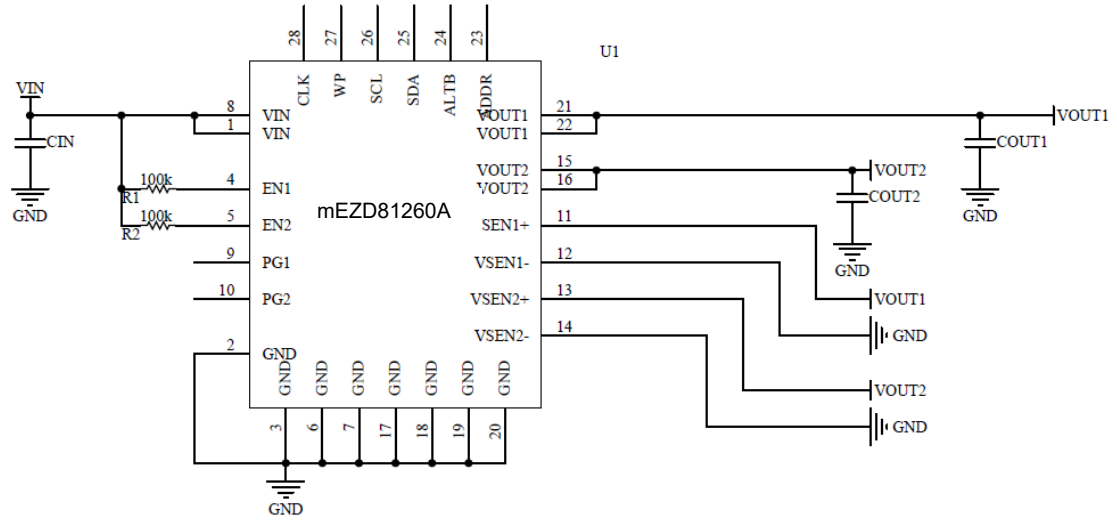
- Wide 5V to 16V Operating Input Range
- 2 Phases or 2 Rails Operation
- 60A Continuous Output Current
- Built-in EEPROM
- PMBus Compliant (Up to 1MHz clock)
- Pin Programmable for PMBus Address (16 addresses)
- Output Voltage Remote Sensing for Both Rails
- Switching Frequency Range 200kHz to 2MHz
- Fast Load Transient Response
- Input voltage, Output voltage and Current, Temperature Monitor
- OVP/UVP/OCP/OTP Protection
- Fault Auto Record Function
- Digital Load and Line Regulation
- Provide Ultrasonic Mode
- EEPROM Write Protection
- Available in LGA-28 (25mm x 15.5mm x 7mm)

APPLICATIONS

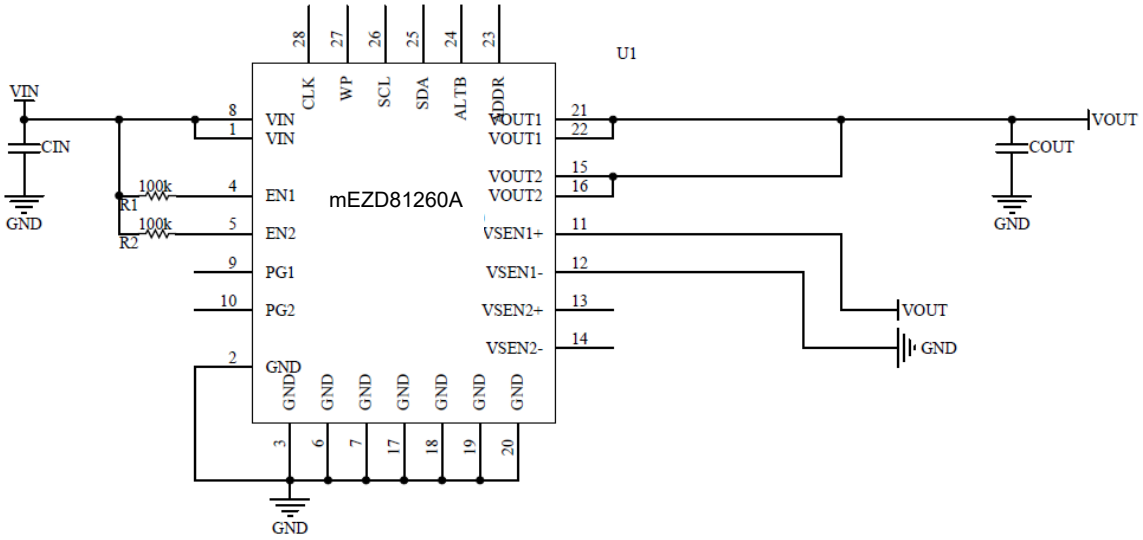
- Power Supplies for Memory,
- DSP, ASIC, FPGA, Microprocessor
- Servers and Storage Equipment
- Industrial / ATE
- Telecom and DATACOM Equipment

TYPICAL APPLICATION

2 Rails:



2 Phases:



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ORDERING INFORMATION

Part Number*	Package	Top Marking
mEZD81260A-xxxx	LGA (25 x 15.5 x 7mm)	*See Below*
EVKT-mEZD81260A-A	\	\
EVKT-mEZD81260A-B	\	\

*For Different Configurations, add suffix –xxxx (e.g. mEZD81260A-0000, it's the default code);

TOP MARKING

MPSYYWW
D81260A
LLLLLLLLL

D81260A: product code of mEZD81260A;
MPS: MPS prefix:
YY: year code;
WW: week code:
LLLLLLLLL: lot number;

EVALUATION KIT EVKT-MEZD81260A-A/B

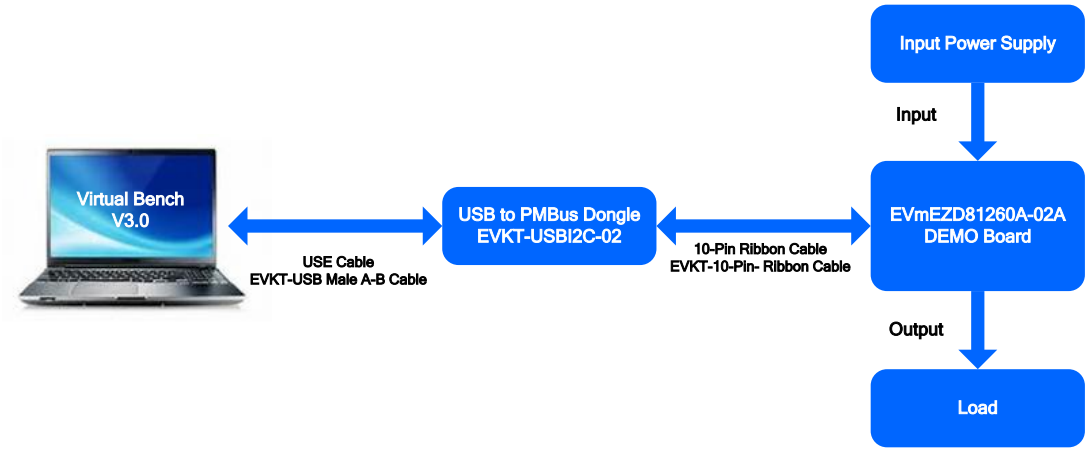
EVKT-mEZD81260A-A Kit contents: (Items can be ordered separately).

#	Part Number	Item
1	EVmEZD81260A-02A-A	mEZD81260A Dual Rails Output Evaluation Board
2	mEZD81260A-0000	1pcs Dual Rails Module
3	EVKT-USBI2C-02*	Includes one USB to I2C Dongle, one USB Cable, and one Ribbon Cable

EVKT-mEZD81260A-B Kit contents: (Items can be ordered separately).

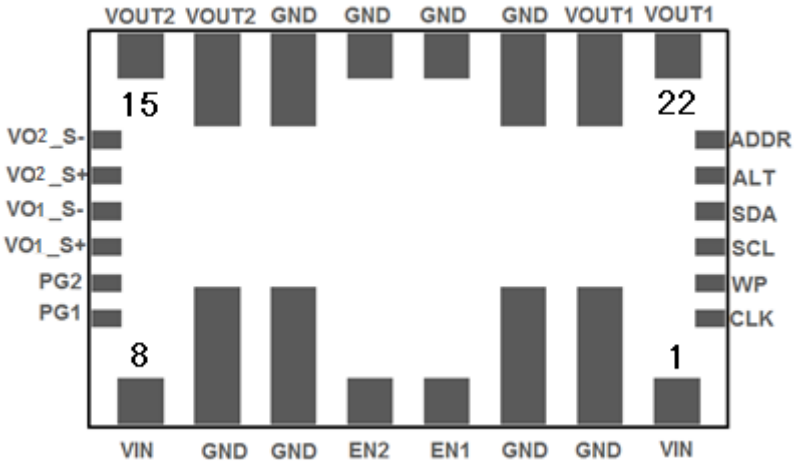
#	Part Number	Item
1	EVmEZD81260A-02A-B	mEZD81260A Dual Phase Single Output Evaluation Board
2	mEZD81260A-0001	1pcs Dual Phase Module
3	EVKT-USBI2C-02*	Includes one USB to I2C Dongle, one USB Cable, and one Ribbon Cable

Order direct from MonolithicPower.com or our distributors



PACKAGE REFERENCE

LGA28(25x15.5x7mm) Standard



Bottom View

ABSOLUTE MAXIMUM RATINGS (1)

V_{IN} ..... -0.3V to 18V
V_{SW} ..... -0.3V to V_{IN}+0.3V (25V for 25ns)

V_{BST} ..... V_{SW}+4V
V_{EN} 4.3V
V_{OUT} 6.5V
V_{PG} 5.5V
All Other Pins ..... -0.3V to 4V
Continuous Power Dissipation (T_A = +25°C) (2) 12W
Junction Temperature ..... 150°C
Lead Temperature ..... 260°C
Storage Temperature ..... -65°C to 150°C

Recommended Operating Conditions (3)

Supply Voltage V_{IN} ..... 5V to 16V
Output Voltage V_{OUT} ..... 0.5V to 3.3V
Operating Junction Temp. (T_J). -40°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JB}

	θ_{JA}	θ_{JB}	
LGA (25x15.5x7 mm)	9	1.5	°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on EVmEZD81260A-01A Demo Board, 6-layer PCB. θ_{JB} is the thermal resistance of MOSFET's junction – module board.

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, T_A = -40°C to +85°C(5), unless otherwise noted. Typical values are at Ta=25°C.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Supply Current (Shutdown)	I_{IN_S}	VEN = 0V			30	mA
Switch Leakage(5)	SW_{LKG}	V_{EN} = 0V, V_{SW} =12V			1	μA
Switching Frequency(5)		Default value	-10%	500	+10%	kHz
High-side Peak Current Limit(5)	I_{LIMIT}	Per phase/rail		50		A
Low-side Negative Current Limit(5)		Per phase/rail		-30		A
Output Voltage Accuracy	V_{REF}	T_A =25°C (Half Load)	-1		1	%
Output Load Regulation	V_{OLDREG}	Vout=1V, Iout=0-30A (Pre rail)	-1		1	%
Output Line Regulation	V_{OLNREG}	Vout=1V, Vin=4.5V-16V (Half Load)	-1		1	%
Output over Voltage Threshold(5)	V_{OVP}	Default Value		115%		V_{REF}
OVP Hysteresis(5)		Default Value		5%		V_{REF}
OVP Delay(5)	T_{OVP}	Default Value		2		μs
Absolute OV Hysteresis(5)				50		mV
PG Rising Threshold(5)	PGH_Rise			95		%
PG Falling Threshold(5)	PGL_Fall			85		%
PG rising delay programmable rage(5)			0		5	ms
Power Good Sink Current Capability	VPG	Sink 12mA			0.6	V
EN Rising Threshold	VEN_RISING		1			V
EN Falling Threshold	VEN_FALL				0.25	V
EN to GND pull-down Resistor	REN			1.1		MΩ
VIN Under-Voltage Lockout Threshold Range	INUVVth	Defaule Value		4.5		V
VIN Under-Voltage Lockout Threshold—Hysteresis	INUVHYS	Defaule Value		500		mV
Soft-Start Time	t_{SS}	Defaule Value		2		ms
Thermal Shutdown (6)		Defaule Value		150		°C
Thermal Hysteresis (6)		Defaule Value		20		°C
Efficiency	Eff	Vout=1V, Io=25A(pre rail)	88	89		%

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, T_A = -40°C to +85°C(5), unless otherwise noted. Typical values are at Ta=25°C.

Parameter	Symbol	Condition	Min	Typ	Max	Units
PMBUS TIMING CHARACTERISTIC AT 400KHZ(5)(6)						
Operating frequency range	f_{SMB}		10		1000	kHz
Bus free time	t_{BUF}	Between stop and start condition	1.3			µs
Holding time	$t_{HD:STA}$		0.6			µs
Repeated start condition setup time	$t_{SU:STA}$		0.6			µs
Stop condition setup time	$t_{SU:STO}$		0.6			µs
Data hold time	$t_{HD:DAT}$		0			ns
Data setup time	$t_{SU:DAT}$		100			ns
Clock low time out	$t_{TIMEOUT}$		25		35	ms
Clock low period	t_{LOW}		1.3			µs
Clock high period	t_{HIGH}		0.6		50	µs
Clock/data fall time	t_F				300	ns
Clock/data rise time	t_R				300	ns
PMBUS TIMING CHARACTERISTIC AT 1MHZ(5)(6)						
Bus free time	t_{BUF}	Between stop and start condition	0.5			µs
Holding time	$t_{HD:STA}$		0.26			µs
Repeated start condition setup time	$t_{SU:STA}$		0.26			µs
Stop condition setup time	$t_{SU:STO}$		0.26			µs
Data hold time	$t_{HD:DAT}$		0			ns
Data setup time	$t_{SU:DAT}$		50			ns
Clock low time out	$t_{TIMEOUT}$		25		35	ms
Clock low period	t_{LOW}		0.5			µs
Clock high period	t_{HIGH}		0.26		50	µs
Clock/data fall time	t_F				120	ns
Clock/data rise time	t_R				120	ns

Notes:

5) Guaranteed by engineering sample characterization.

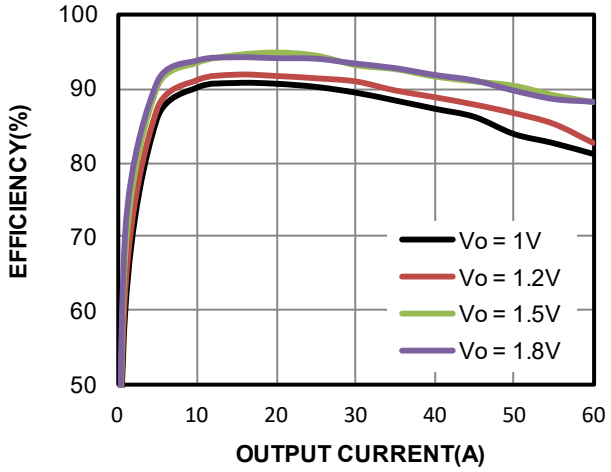
6) Not tested in production and guaranteed by over-temperature correlation.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, V_{OUT} = 1V, T_A = 25°C, unless otherwise noted.

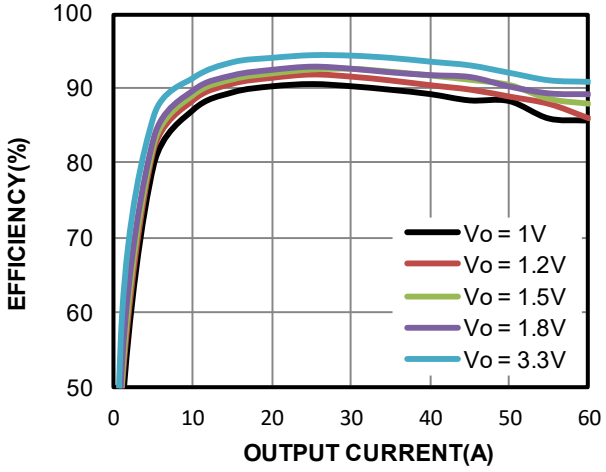
Efficiency

V_{IN}=5V, DUAL PHASE



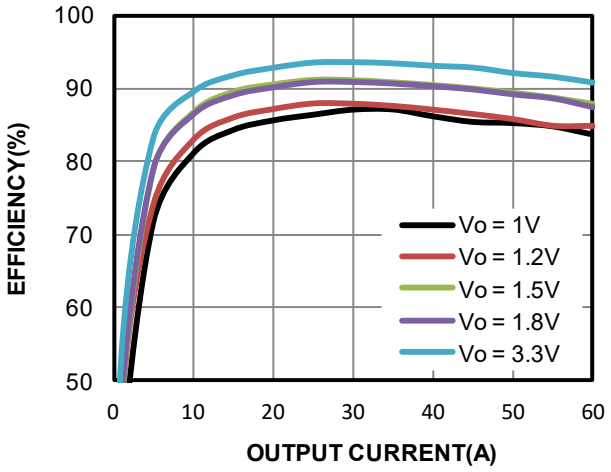
Efficiency

V_{IN}=12V, DUAL PHASE



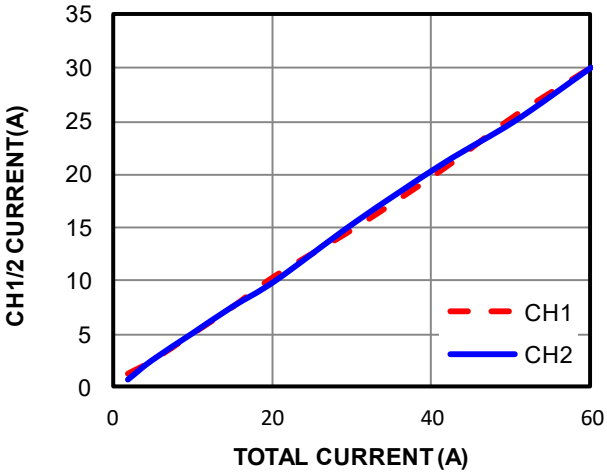
Efficiency

V_{IN}=16V, DUAL PHASE



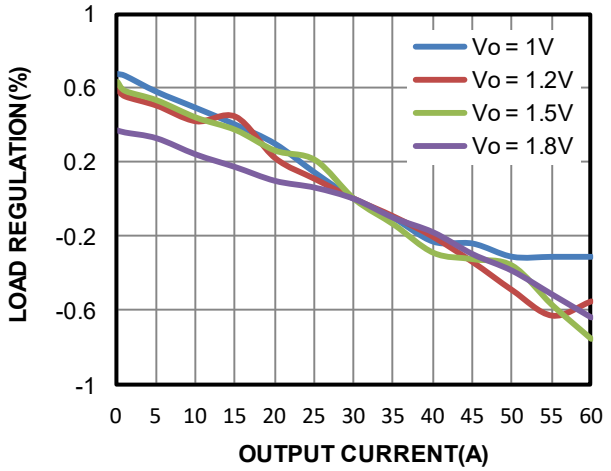
Current Sharing

V_{IN}=12V, I_{OUT}=60A



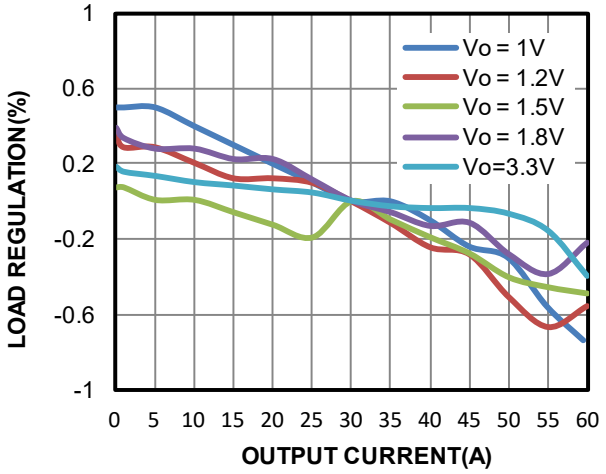
Load Regulation

V_{IN}=5V, DUAL PHASE



Load Regulation

V_{IN}=12V, DUAL PHASE

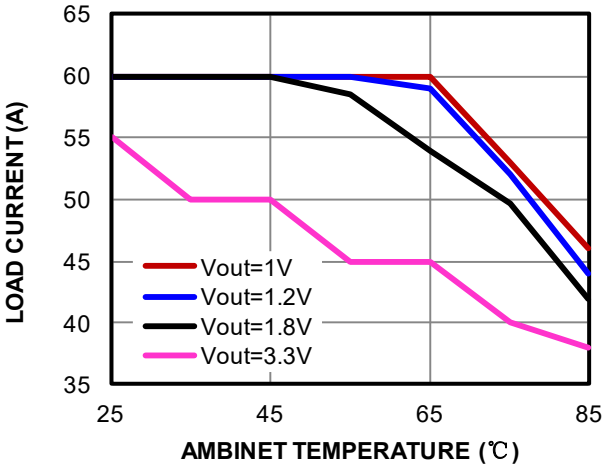


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 1V, T_A = 25°C, unless otherwise noted.

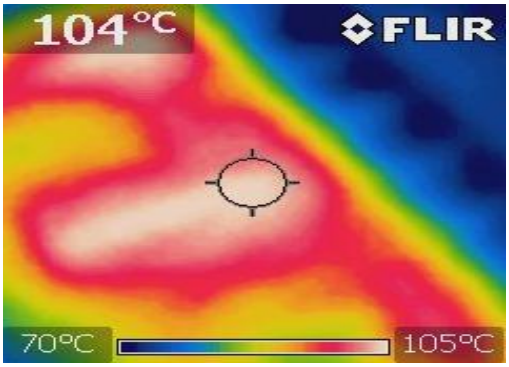
Thermal Derating

Air Flow: 1m/s, V_{IN}=12V



Thermal Image

V_{IN}=12V, V_{OUT}=1V, I_{OUT}=60A

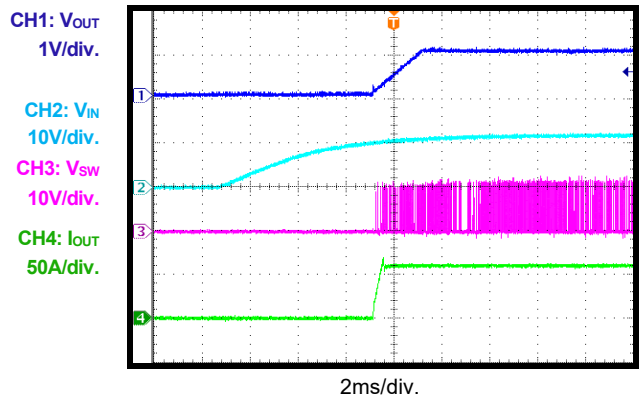


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN}=12V, C_{OUT}=4 x 220µF POSCAP + 20 x 22uF Ceramic, T_A=+25°C, unless otherwise noted.

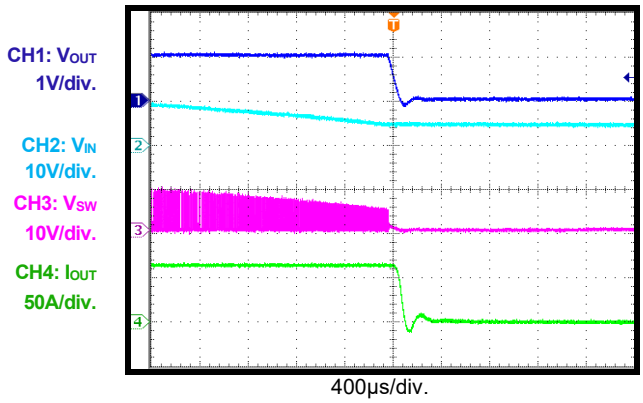
VIN Start-Up, Dual Phase Mode

I_{OUT}=60A



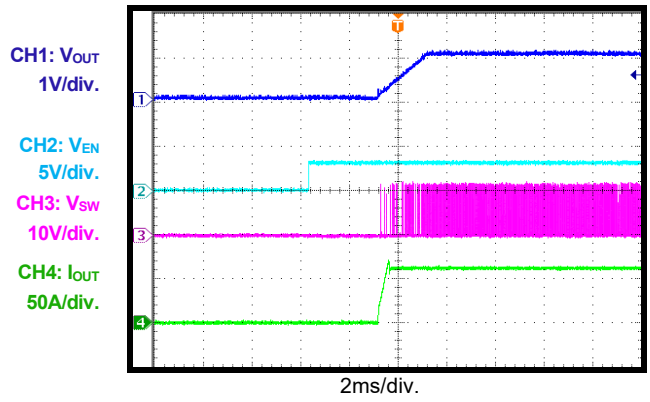
VIN Shutdown, Dual Phase Mode

I_{OUT}=60A



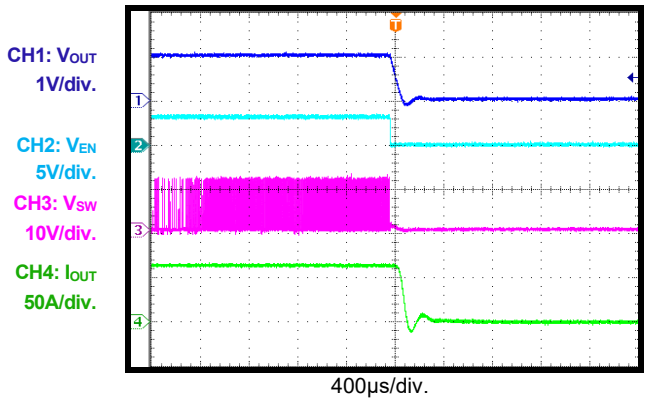
EN Start-Up, Dual Phase Mode

I_{OUT}=60A



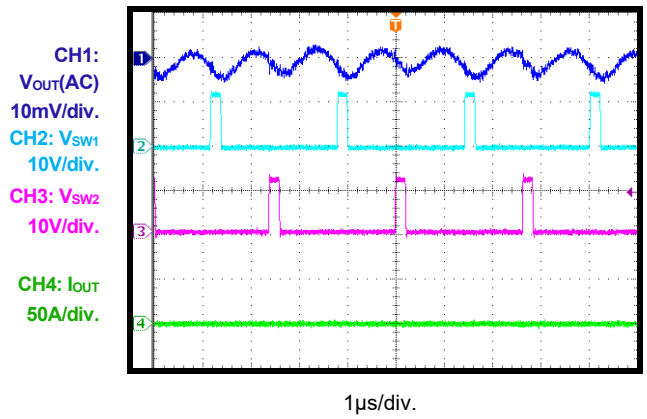
EN Shutdown, Dual Phase Mode

I_{OUT}=60A



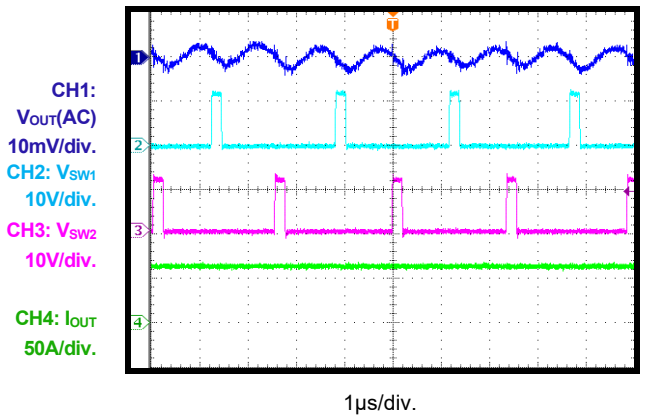
Output Ripple, Dual Phase Mode

I_{OUT}=0A



Output Ripple, Dual Phase Mode

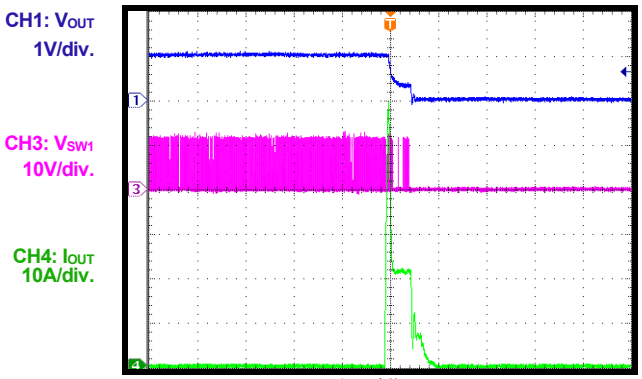
I_{OUT}=60A



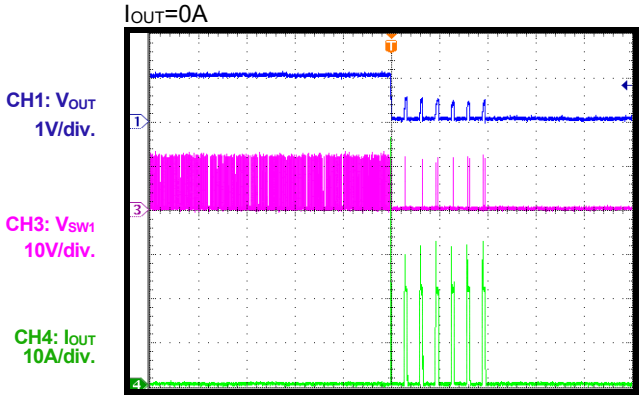
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN}=12V, C_{OUT}=4 x 220µF POSCAP + 20 x 22uF Ceramic, T_A=+25°C, unless otherwise noted.

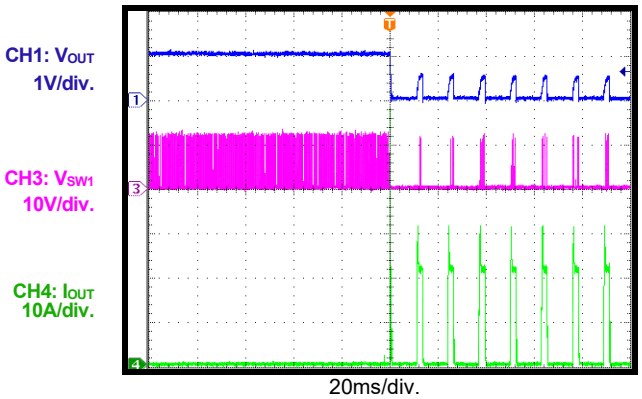
SCP Latch Entry, Dual Phase Mode
I_{OUT}=0A



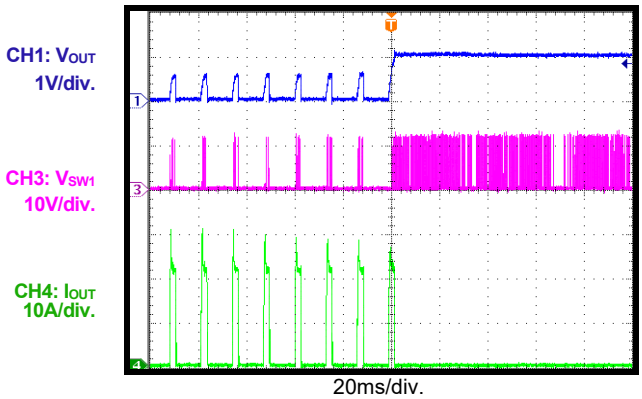
SCP Retry 6 times Entry, Dual Phase Mode
I_{OUT}=0A



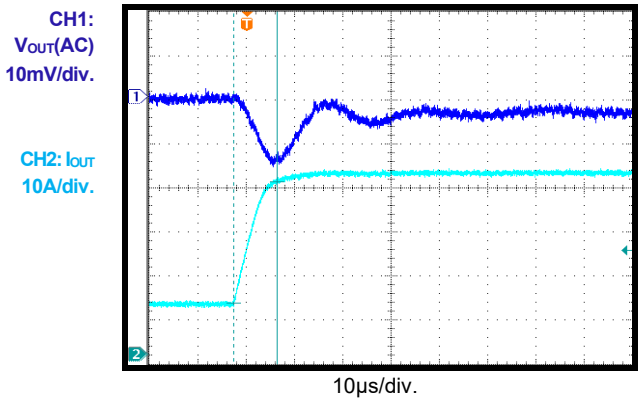
SCP Hiccup Entry, Dual Phase Mode
I_{OUT}=0A



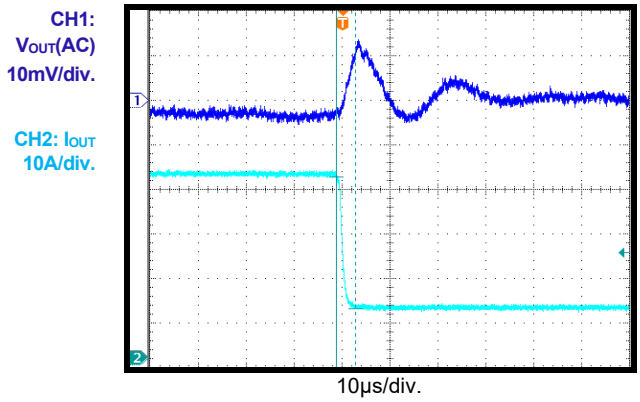
SCP Hiccup Recovery, Dual Phase Mode
I_{OUT}=0A



Transient Response, Dual Phase Mode
10A to 40A



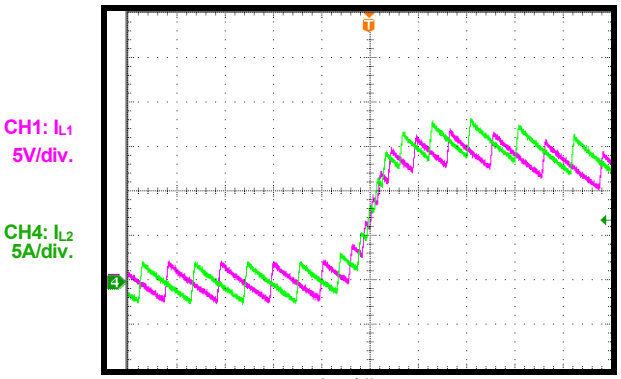
Transient Response, Dual Phase Mode
40A to 10A



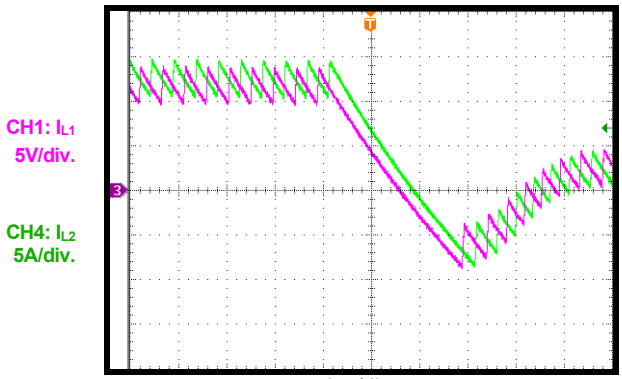
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN}=12V, C_{OUT}=4 x 220µF POSCAP + 20 x 22uF Ceramic, T_A=+25°C, unless otherwise noted.

Current Sharing, Dual Phase Mode
Load Current : 0A to 30A



Current Sharing, Dual Phase Mode
Load Current: 30A to 0A

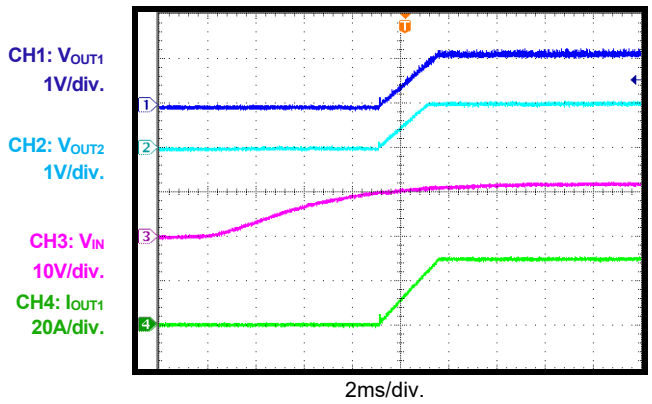


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN}=12V, Per Rail C_{OUT}=2 x 220µF POSCAP + 10 x 22uF Ceramic, T_A=+25°C, unless otherwise noted.

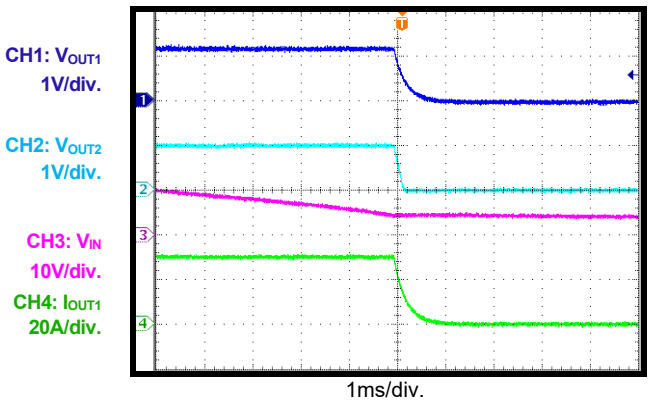
VIN Start-Up, Dual Rail Mode

I_{OUT1}= I_{OUT2}=30A



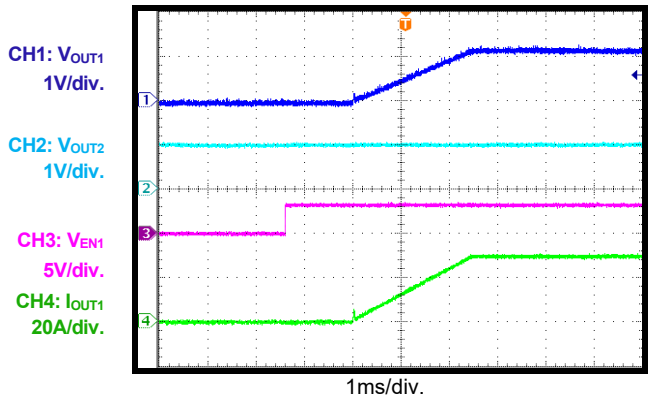
VIN Shutdown, Dual Rail Mode

I_{OUT1}= I_{OUT2}=30A



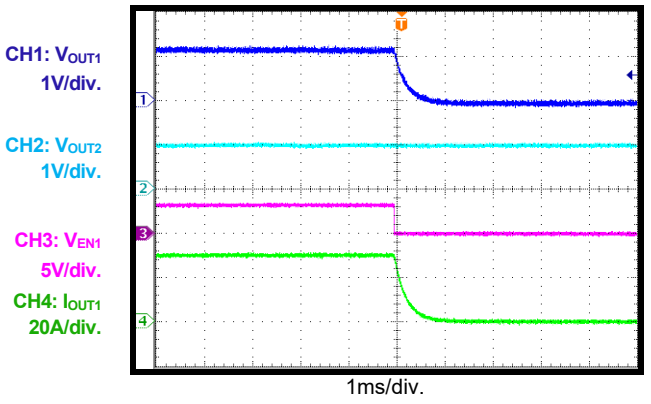
EN1 Start-Up, Dual Rail Mode

I_{OUT1}= I_{OUT2}=30A



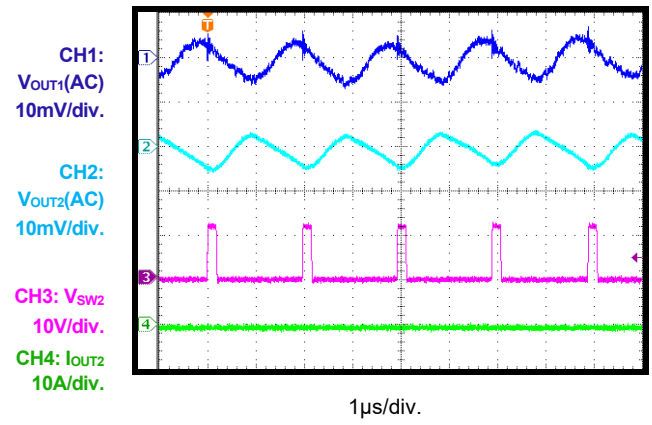
EN1 Shutdown, Dual Rail Mode

I_{OUT1}= I_{OUT2}=30A



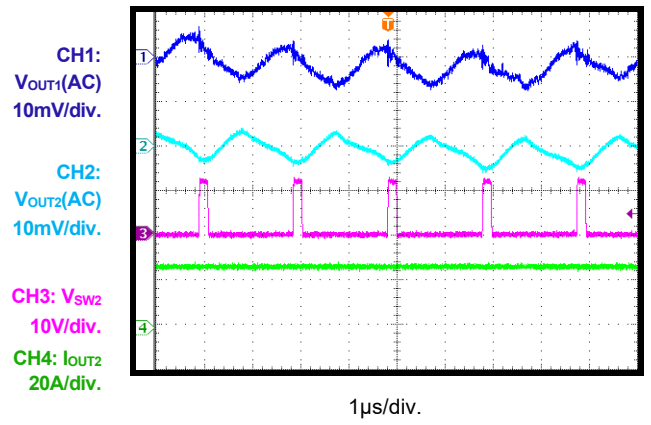
Output Ripple, Dual Rail Mode

I_{OUT1}= I_{OUT2}=0A



Output Ripple, Dual Rail Mode

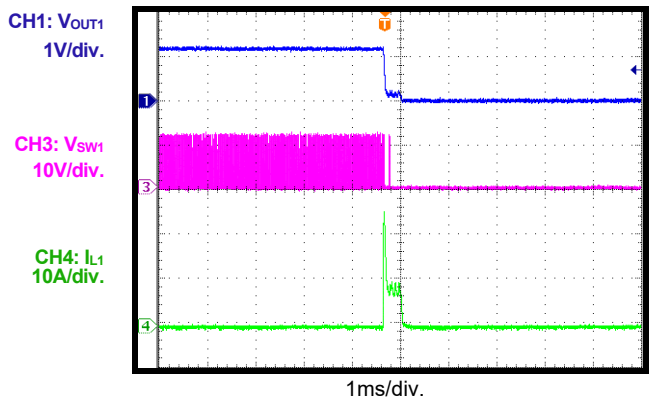
I_{OUT1}= I_{OUT2}=30A



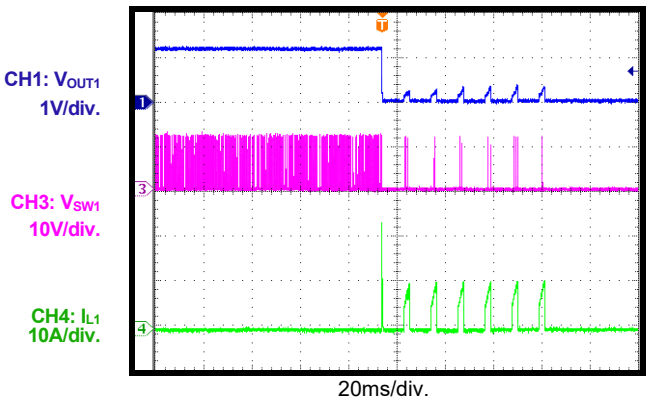
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN}=12V, Per Rail C_{OUT}=2 x 220µF POSCAP + 10 x 22uF Ceramic, T_A=+25°C, unless otherwise noted.

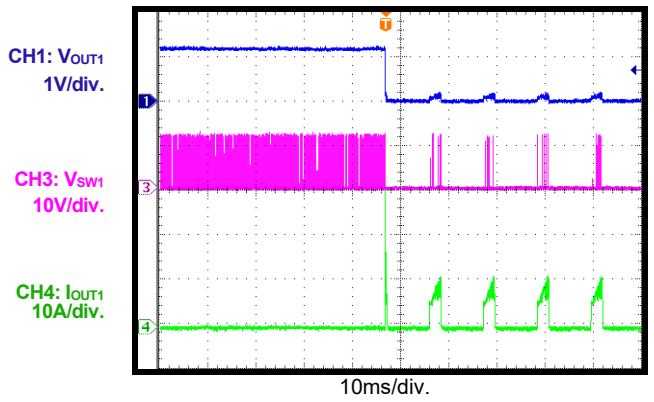
SCP Latch Entry, Dual Rail Mode
I_{OUT1}=0A



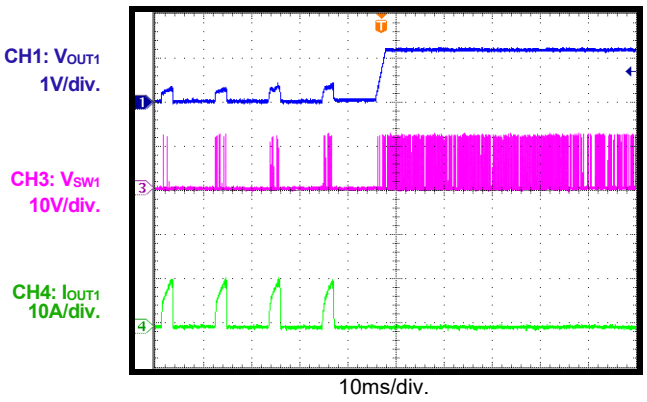
SCP Retry 6 times Entry, Dual Rail Mode
I_{OUT1}=0A



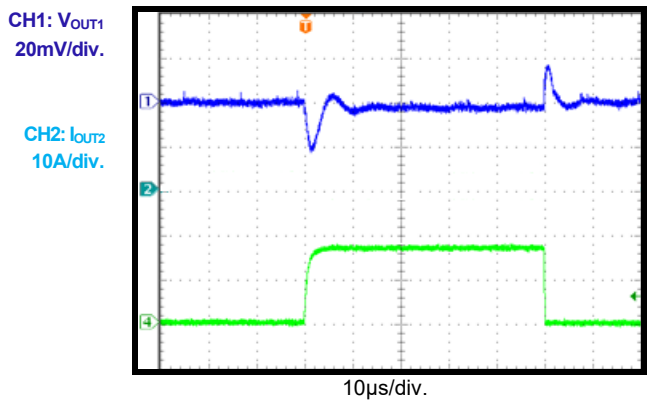
SCP Hiccup Entry, Dual Rail Mode
I_{OUT1}=0A



SCP Hiccup Recovery, Dual Rail Mode
I_{OUT1}=0A



Transient Response, Dual Rail Mode
0A to 15A



PIN FUNCTIONS

Pin #	Name	Description
1,8	VIN	Supply Voltage. The part operates from a 5V to 16V input rail. Requires ceramic capacitor close to module to decouple the input rail. Connect using a wide PCB trace.
2,3,6,7, 17,18,1 9,20	GND	System Ground. Reference ground of the regulated output voltage. Requires special consideration during PCB layout. Connect to GND with copper traces and vias.
21，22	OUT1	Rail1 Power Output pin
15,16	OUT2	Rail2 Power Output pin. Should connect to OUT1 in 2 phase mode.
4	EN1	Rail1 Output enable pin.
5	EN2	Rail2 Output enable pin.
9	PG1	Rail1 Power Good pin. Open drain structure. PG1 switches to open drain state when VOSENSE1>95% VOUT1 Setting and switches to low if <85%.
10	PG2	Rail2 Power Good pin. Open drain structure. PG1 switches to open drain state when VOSENSE2>95% VOUT2 Setting and switches to low if <85%.
11	VO1_S+	Remote Positive Sense pin of rail1 output voltage. Use differential pair to connect to rail1 output capacitor's positive with VO1_S-.
12	VO1_S-	Remote Negative Sense pin of rail1 output voltage. Use differential pair to connect to rail1 output capacitor's positive with VO1_S+.
13	VO2_S+	Remote Positive Sense pin of rail2 output voltage. Use differential pair to connect to rail2 output capacitor's positive with VO2_S-. In 2 phase mode, connect to GND.
14	VO2_S-	Remote Negative Sense pin of rail2 output voltage. Use differential pair to connect to rail2 output capacitor's positive with VO2_S+. In 2 phase mode, connect to GND.
23	ADDR	PMBus address pin. Connect a resistor to GND to choose address. For more information in applications.
24	ALT#	Open drain output that asserts low when a warning has occurred.
25	SDA	Data signal between PMBus controller and mEZD81260A.
26	SCL	Source synchronous clock from PMBus controller.
27	WP	EEPROM Write protection.
28	CLK	SYNC 100kHz clock for the start-up and shut down sequence in multi-rails system. Connect all mEZD81260A CLK together. In single module operation, pull up CLK to 3.3V by 10k resistor. DO NOT LEFT CLK FLOATING.

MODULE SCHEMATIC DIAGRAM

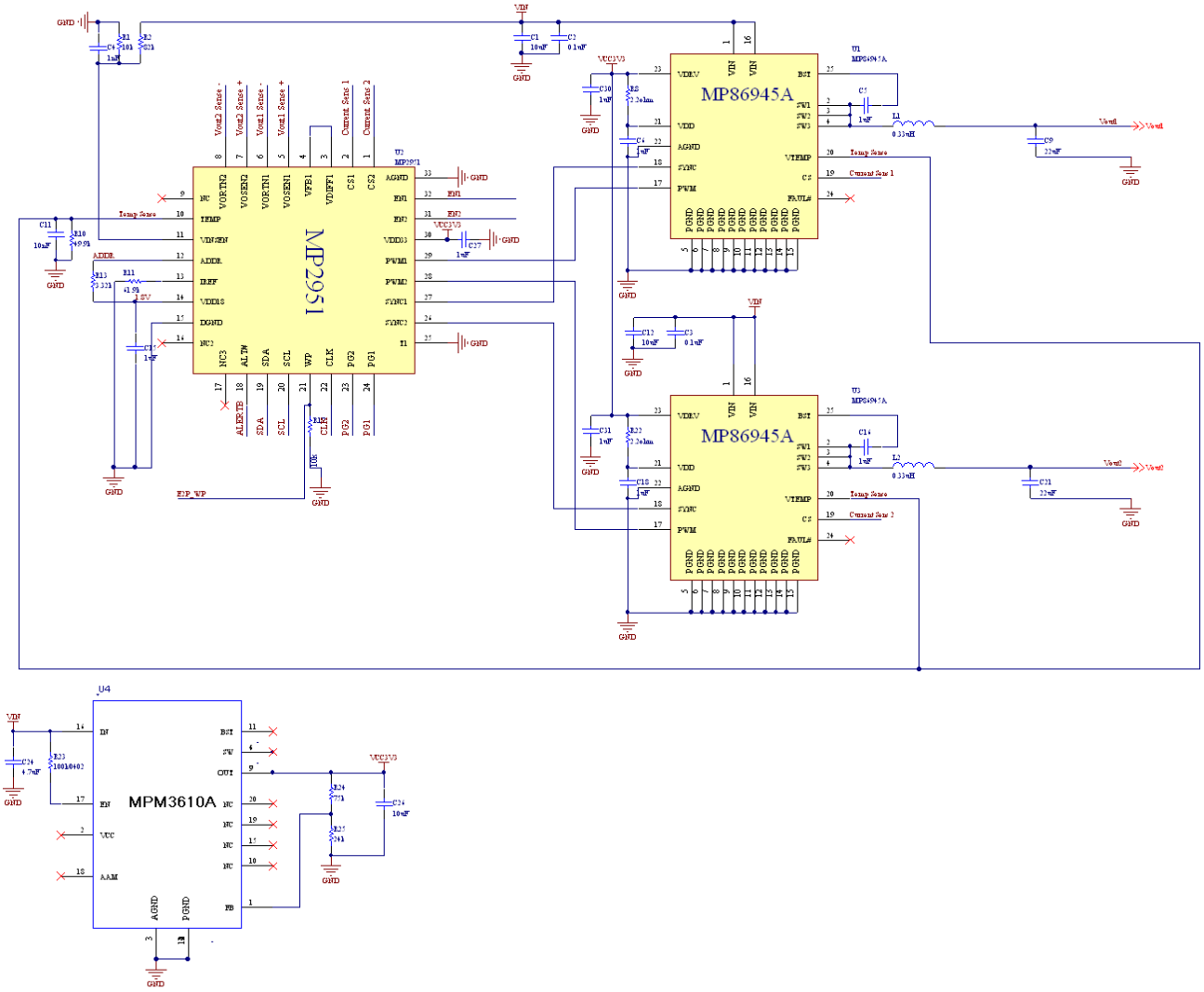


Figure 1: Module Schematic Diagram

OPERATION

The mEZD81260A is a dual rail or dual phase digital DC/DC power module for the POL. Each output can operate independently or be corporate together in the dual phase mode for higher current application.

It adopts a unique loop compensation strategy to balance and optimize the steady and transient performance.

It adopts adaptive phase shedding and phase adding strategy to optimize the overall VR efficiency according to the load current. It contains the blocks of precise DAC and ADC, differential remote voltage sense amplifier, fast comparators, current sense amplifiers, and internal slope compensation.

Rich programmable functions are supported by PMBus interface. Also EEPROM is flexible for custom configuration and auto record the fault type when protection happens.

Fault Protection features include the Vin-UVLO (under voltage lockout), OCP (over current protection), OVP (over voltage protection), UVP (under voltage protection), OTP (over temperature protection) and RVP (reverse voltage protection).

System Configuration

The mEZD81260A provides differential output voltage sense, input voltage sense, and output enable function for both rails. Cooperating with the MPS' Intelli-Phase, the mEZD81260A can sense the real-time phase current and the maximum temperature among the internal power MOSFETs.

The PMBus slave address can be setup by pin configurations or by the registers via PMBus. The mEZD81260A can be configured as 1~2 phase for dual phase mode and 1+1 for dual rail operation application via PMBus.

Soft-Start

Before entering power active state, the mEZD81260A will execute the soft-start process to charge the output capacitor with programmable slow slew rate until the reference reaches the boot voltage. The mEZD81260A provides the TON_DELAY time (configurable from 0s to 6s) before soft-start.

Ultrasonic Mode

The mEZD81260A provides the ultrasonic mode to limit the switching frequency above the 25 kHz at the DCM mode.

When the switching frequency is about 25 kHz, the low-side MOS will be forced turn on to discharge the output cap, when the Vout touches the Vref, the high-side MOS will be turn on and give one Ton shot to charge the Vout up. In this way the switching frequency can be limited to 25 kHz at the light load.

To avoid the double pulse during the ultrasonic mode, patented MPS technology is applied to add the slope compensation to increase the loop regulation stability.

Current balance & Thermal balance loop

The module senses the average value of both phase current and regulates the phase 2 with the current PI loop to achieve the current balance in 2 phase operation.

There is a programmable phase2 current offset which can be used to achieve the thermal balance between the 2 phases. The phase has greater cooling capability because better proximity to airflow can take more phase current by increasing the phase current reference with the offset, so as to keep the phase thermal more balance.

Voltage Reference

The mEZD81260A has two 8-bit VID DAC which provides the reference voltage (V_{REF}) for the individual output. V_{REF} is in VID format with 5mV per step and ranges from 0.25V to 1.52V. Equation (1) shows the relationship between V_{REF} and VID value in decimal:

$$V_{REF}(V) = \begin{cases} 0 & VID = 0 \\ 0.245 + VID \times 0.005 & VID = 1-255 \end{cases} \quad (1)$$

Output Voltage Setting and Sensing

The desired output voltage can be set with PMBus command VOUT_COMMAND (21h). VOUT_COMMAND (21) is a 10-bit register in VID format with 5mV per step. So the output setting range is 0-5.115V. Refer to Register Map/VOUT_COMMAND (21h) section for more information.

The voltage at the load is sensed with unity gain differential voltage sense amplifier for each rail. This type of sensing provides better load regulation.

When VOUT<=1.52V, the maximum reference VID DAC output, connect the remote sense amplifier input pins VOSEN and VORTN to the output at load directly. V_{OUT} equals to V_{REF} at this time.

When V_{OUT}>1.52V, the output voltage must be divided to the reference voltage within 0.25-1.52V. Figure 2 shows the typical connections for V_{OUT}>1.52V and remote sensing is applied.

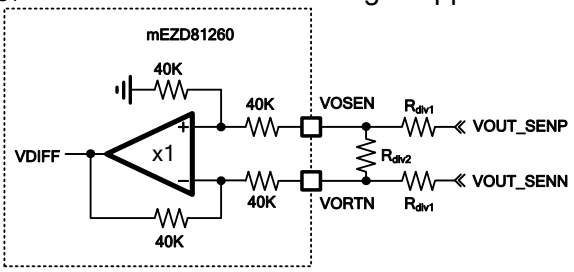


Figure 2. Output Divider Connections when Remote Sense is Applied

VOUT_SENP and VOUT_SENN are from the load and must be routed as a differential pair on quite areas. Use equation (2) to calculate the voltage divider ratio in Figure 2.

$$K_R = \frac{V_{DIFF}}{V_{OUT}} = \frac{1}{(\frac{1}{R_{div1}} + \frac{2}{R_{div2}} + \frac{1}{40K}) \times R_{div1}} \quad (2)$$

The K_R must be programmed into the mEZD81260A by PMBus command VOUT_SCALE_LOOP (29h) with equation (3). The controller uses it to determine the reference voltage.

$$VOUT\_SCALE\_LOOP = 2^7 \times K_R \quad (3)$$

Where

VOUT_SCALE_LOOP is the programmed value in register VOUT_SCALE_LOOP (29h).

Equation (4) shows the reference voltage calculation in the mEZD81260A. Be noted that the reference voltage is in 5mV per step. The value besides this step is dropped. To minimize the output voltage DC setting error, match the real output divider ratio by R_{DIV1} and R_{DIV2} and PMBus setting ratio by command VOUT_SCALE_LOOP (29h) well, and design a VREF close to multiples of 5mV.

$$V_{REF} = \frac{VOUT\_SCALE\_LOOP}{2^7} \times V_{OUT} \quad (4)$$

Refer to Register Map/VOUT_SCALE_LOOP (29h) section for more information.

To prevent output voltage out of regulation, ensure the voltage on VOSEN pin is lower than the maximum allowed sensing voltage (2.9V) at any time.

For output voltage designs above the VOSEN pin specification, connect the output divider as shown in Figure 3. VORTN is connected to GND directly to disable remote sensing.

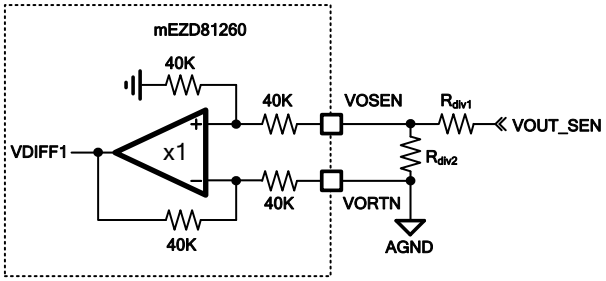


Figure 3 Output Divider Connections when Remote Sense is not Applied

Use equation (5) to calculate the voltage divider ratio in Figure 3.

$$K_R = \frac{V_{DIFF}}{V_{OUT}} = \frac{1}{(\frac{1}{R_{div1}} + \frac{1}{R_{div2}} + \frac{1}{80K}) \times R_{div1}} \quad (5)$$

Table 1 shows the recommended output divider resistors and PMBus register settings for typical POL output voltages. Table 1-a shows the resistor values in Figure 4 when remote sensing is applied. Table 1-b shows the resistor values in Figure 3 when remote sensing is disabled.

Table 1-a Recommended Output Divider with Remote Sensing

V_{OUT} (V)	R_{div1} (KΩ)	R_{div2} (KΩ)	K_R	VOUT_SCALE_LOOP (29h)	V_{REF} (V)
0.8	0	NS(8)	1	0x0080	0.8
1	0	NS	1	0x0080	1
1.2	0	NS	1	0x0080	1.2
1.5	0	NS	1	0x0080	1.5
3.3	3.01	2.05	0.25	0x0020	0.825

Table 1-b Recommended Output Dividers without Remote Sensing

V_{OUT} (V)	R_{div1} (KΩ)	R_{div2} (KΩ)	K_R	VOUT_SCALE _LOOP (29h)	V_{REF} (V)
0.8	0	NS	1	0x0080	0.8
1	0	NS	1	0x0080	1
1.2	0	NS	1	0x0080	1.2
1.5	0	NS	1	0x0080	1.5
3.3	6.04	2.05	0.25	0x0020	0.825

Note: (8) NS means not stuffed.

The mEZD81260A provides high resolution trimming and digital DC calibration to attain output voltage setting accuracy within +/-5mV/K_R.

The digital DC calibration can be enabled with PMBus command MFR_VR_CONFIG (D0h), bit [10:7]. Refer to Register Map/ MFR_VR_CONFIG (D0h) section for more information.

Input Voltage Sense

The input power supply voltage is sampled by a internal resistor divider and it is used for the output voltage regulation as the feed-forward control, Vin_UVLO, Vin_OVP fault protection, and monitoring via PMBus. Same as the output voltage sense, input voltage sense also has the MFR_VIN_SCALE_LOOP command for presenting the ratio of input voltage divider.

Current Sense

The phase currents are sampled by the ADC and then convert to the direct current format (0.5A/LSB) in the module.

The mEZD81260A has a compensation circuit for the phase current sense to obviate the current sense drifts at the different part or temperature condition.

Current balance & Thermal balance loop

The mEZD81260A provides a current balance loop to achieve the fair current sharing at dual phase mode when different circuit impedance leads to a phase current difference. The mEZD81260A provides a current balance function enable bit in PMBus command MFR_VR_FIG (D0h) at dual phase mode. It is disabled automatically at dual rail mode.

Refer to PMBus Register Map / MFR_VR_FIG (D0h) section for more information.

At dual phase mode, there is a programmable phase2 current offset which can be used to achieve the thermal balance between the 2 phases. The phase which has greater cooling capability because of better proximity to airflow can take more phase current by increasing the phase current reference with the offset, so as to keep the thermal in balance between phases.

Refer to PMBus Register Map / MFR_CS_OFFSET (D1h) for more information.

Temperature Sense

The mEZD81260A senses the internal driver MOSFET's temperature, which is the highest temperature of the power system. The sensed temperature is used for over temperature fault protection.

Dynamic Voltage Identification (DVID)

The MEZD81260A supports dynamic output voltage transition by changing VID code with the PMBus commands: VOUT_COMMAND (21h), MARGIN-HIGH (25h), and MARGIN-LOW (26h). The DVID is active after the V_{OUT} is settled. The V_{OUT} change can be either upwards or downwards stepping. The DVID slew rate is set with PMBus command TOFF_FALL (65h).

The reference voltage transition slew rate ranges from 0.012-50mV/us.

Refer to PMBus Register Map/ TOFF_FALL (65h) section for more information.

When a VID transition occurs, PG signal keeps asserting except the sensed output voltage on VDIFF is lower than 85% of VREF.

During a VID transient, the controller pull forces the VR into full phase CCM mode regardless the power state setting. For example, it means that if the controller is configured as a dual phase mode but it is running in 1-phase DCM due to auto power mode and a light load condition, a VID transition command will lead the controller run into 2-phase CCM immediately by pulling both SYNC1 and SYNC2 high.

Operation of EEPROM

The mEZD81260A provides EEPROM to store custom configurations. A 4-digital part number suffix is assigned for each application. The default configuration values for each 4-digital part can be pre-programmed at the MPS factory. The

data can program again using STORE_USER_ALL (15h) command via PMBus. EEPROM will be read automatically during power on sequence or by the RESTORE_USER_ALL (16h) command via PMBus.

The operation of the EEPROM can be easily accomplished with the MPS GUI software.

The mEZD81260A has two ways (hardware or software) to enable EEPROM write protection.

1. pull WP pin high to 3.3V with a 4.99 KΩ resistor.
2. set register MFR_EEPROM_WP (DBh) ≠ 0x63.

The EEPROM is abled to be erased/writed more than 100,000 cycles. When EEPROM is write-protected, the write into EEPROM actions is in-effective.

Power on

The mEZD81260A will be reset by the internal power-on reset signal (POR) after VIN supply is ready and either EN1 or EN2 asserts. After system comes out of POR, the data in EEPROM is loaded into the operating registers to configure the POL operation.

Figure 4 shows the power on sequence of the mEZD81260A.

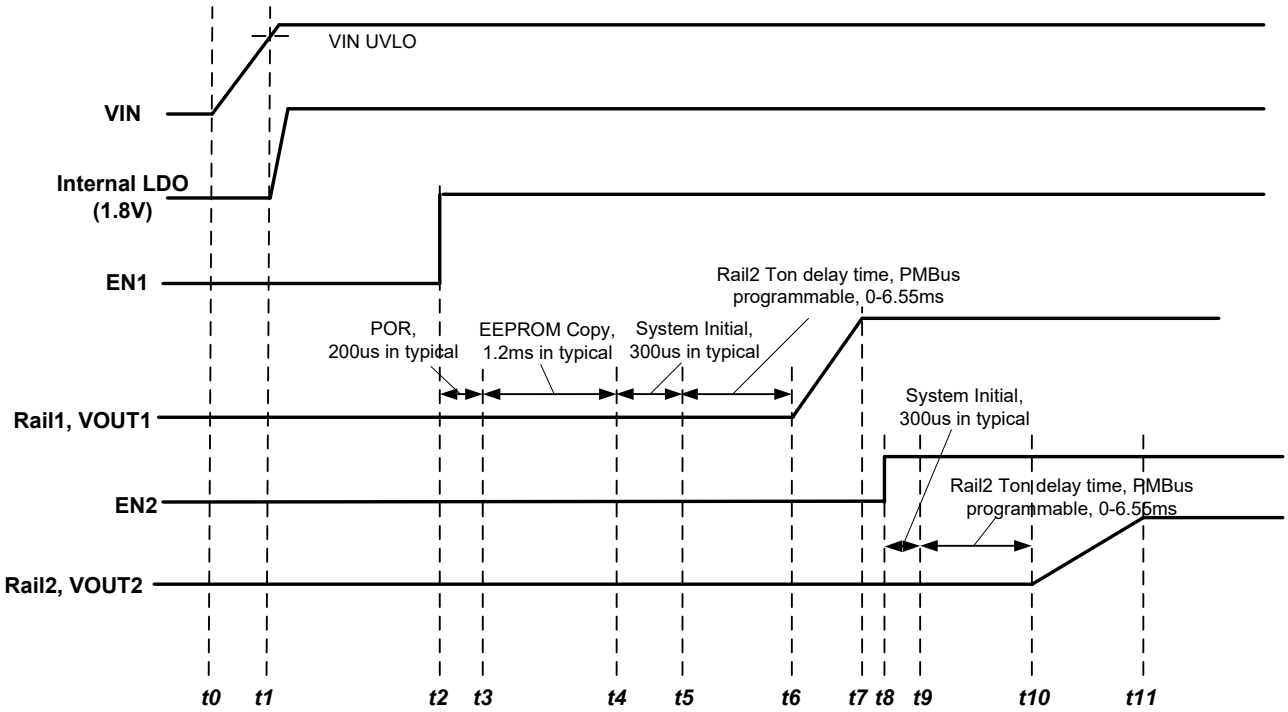


Figure 4 mEZD81260A Power On Sequence

t0~t1: VIN reaches the UVLO on threshold at t1.

t1~t2: when Vin rising above UVLO on threshold, the internal LDO starts building 1.8V voltage. After 1.8V is ready, and before either EN1 or EN2 pulls high, the module works in low power consumption mode. VIN consumes less than 30mA current when both EN pin pulls low. The internal digital blocks is not active at this state. It means EEPROM is not accessible.

t2~t3: at t2, EN1 is pulled high, a 200us POR process starts and ends at t3. Be noted either EN1 or EN2 can starts the POR and power on process. In Figure 4, it takes EN1 pull-high firstly as an example.

t3~t4: at t3, the data in EEPROM starts loading into operating registers. It is also referred as EEPROM copy. The entire EEPROM copy process takes about 1.2ms in typical.

t4~t5: after EEPROM copy is finished, the module begins system initialization to configure rail1 POL operations. During this stage, the PMBus address is detected if user selects the voltage on ADDR pin to set the PMBus address. After that users are able to scan the PMBus

address by MPS GUI. The system initialization lasts for about 300us in typical.

t5~t6: after system initialization, if the rail1 PMBus command OPERATION (01h, page0) is pre-set to 'off' state. The module will halt at this stage and wait for an OPERATION on command. If the OPERATION (01h, page1) is pre-programmed to "on" state, rail1 turn-on delay time (Ton delay) starts counting. Ton delay time is PMBus programmable from 0 to 6.55ms with command TON_DELAY (60h, page0). Refer to Register Map section for more information.

t6~t7: when Ton delay time expires, rail1 VID DAC starts ramping up the VREF1 with programmed slew rate. This is called soft-start. During soft-start, OCP-Total protection, OVP and UVP are masked until the VREF1 reaches target value. If the MEZD81260A is programmed to dual phase mode, the power on sequence is completed at t7. Rail1 is ready to output power to the load, do DVIDs and take other power actions after t7.

t8~t9: at dual rail mode, rail2 is controlled by EN2 signal. When EN2 asserts, rail2 begins system initialization to configure its POL operations. The system initialization takes about 300us in typical.

t9~t10: after rail2 system initialization, when OPERATION (01h, page1) is set to command on, rail2 Ton delay time initiates. Ton delay of rail2 is also PMBus programmable with command TON_DEALY (60h, page1).

t10~t11: at t10, when Ton delay time expires, rail2 VID DAC output starts ramping up VREF2. This is the soft-start process of rail2. At t11, the power on sequence of both rails is completed.

Power off

The mEZD81260A can be powered off by operation command, EN pins or VIN voltage:

1. Operation command off: the module provides high-Z off and soft-off with operation command off. When the OPERATION command is set to soft off, the VOUT will soft shut down with the pre-programmed slew rate as in the register TOFF_FALL (65h). A turn-off delay (Toff delay) can be added via PMBus command TOFF_DELAY (64h) at OPERATION command soft off.
2. EN off: when pull down the EN1 pin, the rail1 starts high-Z shutting down; when pull down the EN2 pin, then the rail2 starts high-Z shutting down. After both EN1 and EN2 pins pulls low, the module enters standby mode with smallest power consumption. EEPROM is not accessible anymore. The internal controller can restart by pulling up either EN1 or EN2 pin.
3. VIN power off: when the voltage supply on VIN pin falls below the UVLO falling threshold, the module output is powered off immediately.

Figure 5 shows an operation command off on rail1 and EN off on rail2.

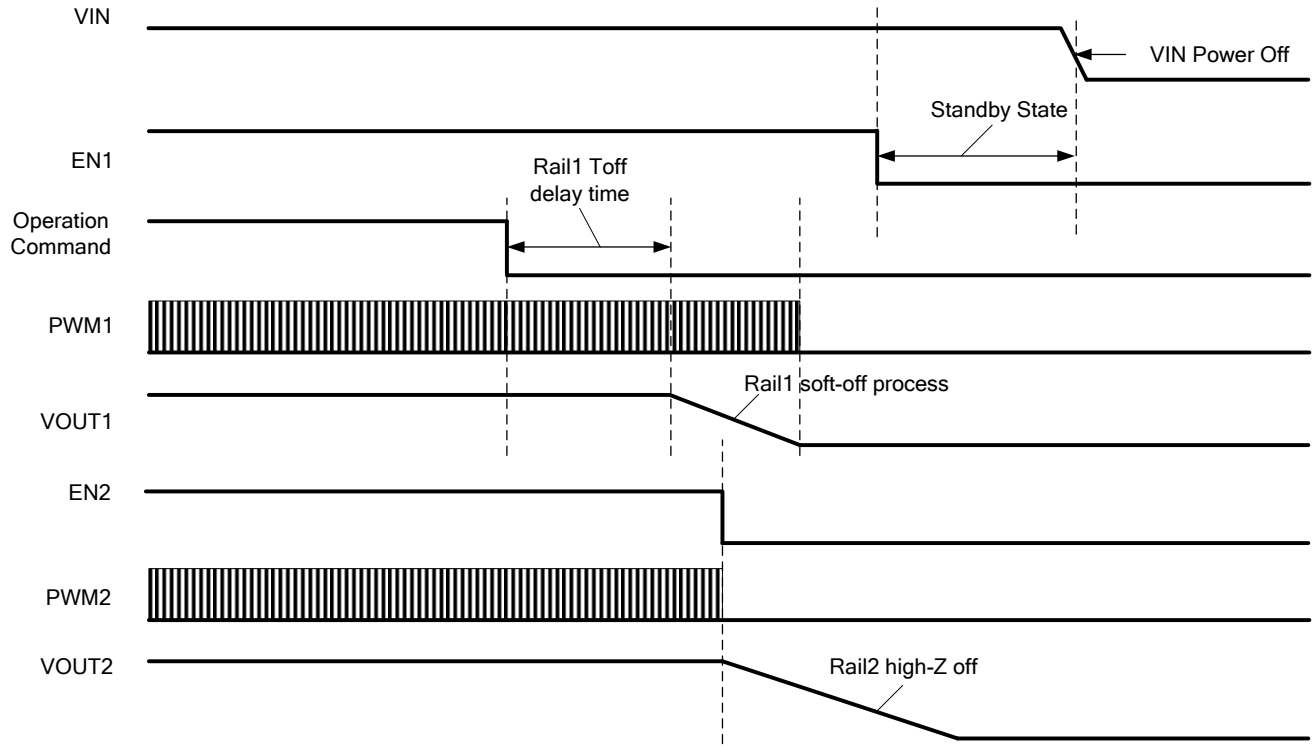


Figure 5 mEZD81260A Power Off Sequence

Power Good Indication

The module provides individual PG pins for both rails. It monitors the voltage on VFB to indicate whether the output voltage is in regulation. For rail2, VFB is the internal output of remote sense amplifier. During the soft-start sequence, the PG de-asserts initially. When the VFB voltage reaches 95% of target VREF, PG asserts after a PMBus programmable PG on delay time. After the output is in regulation, PG de-asserts immediately once VFB falls below 85% of VREF.

At OPERATION command soft off state, PG de-asserts once VFB falls below 85% of steady state.

At fault protections, OPERATION command high-Z off or EN power off, PG indicates low immediately without delay.

Figure 6 shows the PG indication at different state.

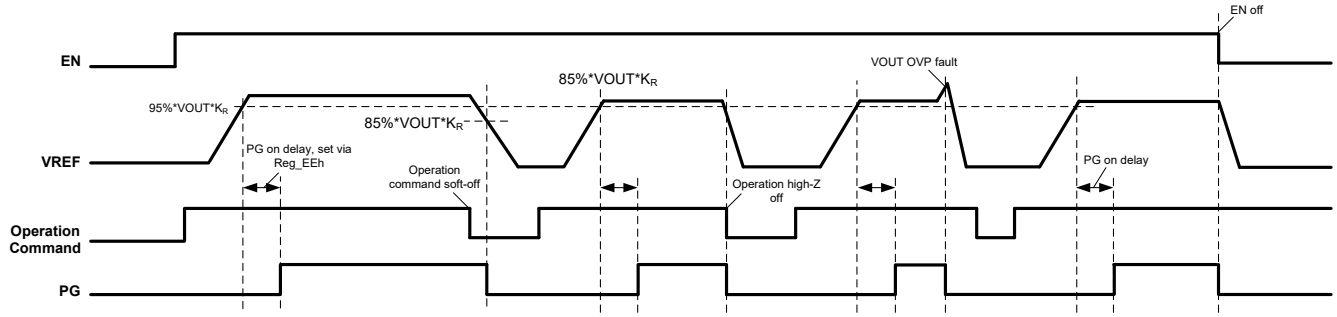


Figure 6 Power Good Indication

PMBUS COMMUNICATION

General Description

The Power Management Bus (PMBus) is an open standard power-management protocol that defines a means of communicating with power conversion and other devices. It is a two-wire, bidirectional serial interface, consisting of a data line (SDA) and a clock line (SCL). The lines are externally pulled to a bus voltage when they are “idle”. Connecting to the line, a master device generates the SCL signal and device address and arranges the communication sequence. It is based on the principles of operation of I2C.

The mEZD81260A supports 100KHz, 400KHz and 1MHz bus timing requirements. Timing and electrical characteristics of the PMBus can be found in the Electrical Characteristics section or in the PMB Power Management Protocol Specification, part1, revision 1.3 available at http://PMBus.org.

PMBus Address

To support multiple VR devices used with the same PMBus interface, the mEZD81260A provides PMBus address programming either by ADDR pin or by register MFR_ADDR_PMBUS (EDh, page0).

The PMBus address is a 7-bit code and ranges from 0x00 to 0x7F. The 3MSB bit is set by the register. The 4LSB bit address can be either set by the register or by the ADDR voltage.

The address of 00h is reserved as the PMBus all call address. Don’t set it as the mEZD81260A unique PMBus address.

Register MFR_ADDR_PMBUS (EDh, page0) is used to program or store the PMBus address. Bit [7] sets the PMBus address 4LSB bit configuration mode. When bit [7]=0, the 4LSB bit is determined by ADDR voltage and stored in register EDh bit [3:0].

The ADDR voltage can be programmed by a resistor from the ADDR to GND. Figure 7 shows the recommended connections for ADDR pin. Taking the 3MSB bit is set to 3’b010 as an example. Table 2 shows the resistor values for different PMBus addresses.

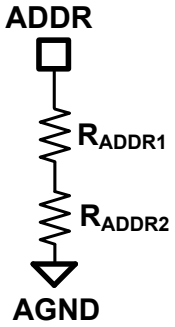


Figure 7 Recommended Circuit Design of ADDR

Table 2 Pin Configuration for PMBus Address

PMBus Address	Setting Point(V)	R_{ADDR1} (kΩ) 1%	R_{ADDR2} (Ω) 1%
20h	0	0	Short
21h	0.034	1.74	Short
22h	0.059	3	Short
23h	0.086	4.32	40.2
24h	0.118	5.9	93.1
25h	0.157	7.87	110
26h	0.207	10.2	316
27h	0.267	13.3	237
28h	0.340	16.9	365
29h	0.430	21.5	330
2Ah	0.539	27	350
2Bh	0.673	34	178
2Ch	0.841	42.2	510
2Dh	1.045	52.3	768
2Eh	1.296	64.9	910
2Fh	1.706	86.6	Short

Data and Numerical Format

The mEZD81260A uses the direct format internally to represent real-world value such as voltage, current, power, temperature, time, etc.

All numbers with no suffix in this document are decimal unless explicitly designated otherwise.

Numbers in binary format are indicated by a prefix “n’b”, where n means the binary count. For example, 3’b000 means it is a 3-bit binary data, and the data is 000.

The suffix “h” indicates hexadecimal format, which is generally used for the register address number in this document.

The symbol “0x” indicates hexadecimal format which is used for the value in the register; for

example 0x88 is 1byte number whose decimal value is 136.

PMBus Communication Failure

A data transmission fault occurs when the data is not properly transferred between the devices. There are several data transmission faults. All sorts of faults are listed below.

- Sending too few data
- Reading too few data
- The master sends too many bytes
- The mEZD81260A reading too many bytes.
- Improperly set read bit in the address byte
- Unsupported command code

The data transmission faults will assert ALT_P#. The CLEAR_FAULTS (03h) command will de-assert ALT_P#, but if the faults still exist, ALT_P# will assert again.

PMBUs Reporting and Status Monitoring

The mEZD81260A supports real time monitor for the VR operation parameters and status with the PMBus interface.

Table 3 lists the monitored parameters.

Table 3 PMBus Monitored Parameters

Parameter	PMBus
Output Voltage	3.13mV/LSB
Output Current	0.5A/LSB
Temperature	1°C/LSB
Input Voltage	0.25V/LSB
Phase Current	0.5A/LSB
V_{OUT} OV Fault	√
V_{OUT} UV Fault	√
OC Fault	√
OT Fault	√
V_{IN} UVLO Fault	√
V_{IN} OVP Fault	√
PMBus Fault	√
EEPROM Fault	√

Supported PMBUS Commands

Command Code	Command Name	Type	Bytes	Page 0 (Rail1)	Page1 (Rail2)
00h	PAGE	r/w	1	√	√
01h	OPERATION	r/w	1	√	√
02h	MFR_CLK_MASTER	r/w	1	√	
03h	CLEAR_FAULTS	send	0	√	√
15h	STORE_USER_ALL	send	0	√	√
16h	RESTARE_USER_ALL	send	0	√	√
21h	VOUT_COMMAND	r/w	2	√	√
22h	VOUT_TRIM	r/w	2	√	√
25h	VOUT_MARGIN_HIGH	r/w	2	√	√
26h	VOUT_MARGIN_LOW	r/w	2	√	√
29h	VOUT_SCALE_LOOP	r/w	2	√	√
33h	FREQUENCY_SWITCH	r/w	2	√	√
35h	VIN_ON	r/w	2	√	
36h	VIN_OFF	r/w	2	√	
55h	VIN_OV_FAULT_LIMIT	r/w	2	√	
60h	TON_DELAY	r/w	2	√	√
61h	TON_RISE	r/w	2	√	√
64h	TOFF_DELAY	r/w	2	√	√
65h	TOFF_FALL	r/w	2	√	√
86h	MFR_FAULTS	r	2	√	
87h	MFR_CML	r	1	√	
88h	READ_VIN	r	2	√	
8Bh	READ_VOUT	r	2	√	√
8Ch	READ_IOUT	r	2	√	
8Dh	READ_TEMPERATURE	r	2	√	
8Fh	MFR_CS	r	1	√	√
D0h	MFR_VR_CONFIG	r/w	2	√	
D4h	MFR_VIN_SCALE_LOOP	r/w	1	√	
D6h	MFR_OCP_TOTAL_SET	r/w	2	√	√
D7h	MFR_OVP_SET	r/w	2	√	√
D8h	MFR_UVP_SET	r/w	2	√	√
D9h	MFR_OTP_SET	r/w	2	√	
DAh	MFR_OCP_PHASE_SET	r/w	2	√	√
DBh	MFR_PRT_RETRYTIME	r/w	1	√	
	MFR_EEPROM_WP				√
DCh	MFR_PRT_CONFIG	r/w	1	√	
E1h	MFR_BLANK_TIME	r/w	1	√	
	MFR_MIN_OFF_TIME				√
E2h	MFR_SLOPE_SR_PS0	r/w	2	√	
E3h	MFR_SLOPE_CNT_PS0	r/w	1	√	

Supported PMBUS Commands *(Continue)*

Command Code	Command Name	Type	Bytes	Page 0 (Rail1)	Page1 (Rail2)
E4h	MFR_SLOPE_SR_PS1	r/w	1	√	√
E5h	MFR_SLOPE_CNT_PS1	r/w	2	√	√
E6h	MFR_SLOPE_SR_PS2	r/w	1	√	√
E7h	MFR_SLOPE_CNT_PS2	r/w	1	√	√
EAh	MFR_SLOPE_SR_F25K	r/w	1	√	√
EBh	MFR_PS01_TRIM	r/w	2	√	
	MFR_PS1_TRIM				√
ECh	MFR_PS23_TRIM	r/w	2	√	√
EDh	MFR_ADDR_PMBUS	r/w	1	√	
EEh	MFR_PG_RDL	r/w	2	√	√
EFh	VENDOR_ID	r/w	1	√	
F0h	PRODUCT_ID	r/w	1	√	
F1h	PRODUCT_REV_VR	r/w	1	√	
F2h	MFR_PSI_SET	r/w	1	√	√
F3h	MFR_PSI_ENTER	r/w	2	√	√
F4h	MFR_PS_HYS	r/w	1	√	√
F6h	MFR_SAMP_LPF	r/w	1	√	
F7h	MFR_VR_CONFIG_ADV	r/w	2	√	
F8h	MFR_FAULTS_RECORD	r	2		√
F9h	MFR_DRMOS_TYPE	r/w	2	√	
FFh	CLEAR_EEPROM_FAULTS	send	0	√	√

Page0 Register Map

PAGE (00h)

The PAGE command provides the ability to configure, control and monitor through only one physical address for both rails and the test mode.

Command	PAGE							
Format	Unsigned binary							
BIT	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	X	X	PAGE	

Bits	Bit Name	Description
7:2	RESERVED	Unused. X indicates writes are ignored and always read as 0.
1:0	PAGE	2’b00: Page0, all commands address rail1 2’b01: Page1, all commands address rail2 Others: In-effective input

OPERATION (01h)

The OPERATION command on page0 is used to turn the rail1 output on/off in conjunction with input from the EN1 pin. It is also used to set the output voltage to the upper or lower MARGIN voltages. The rail1 stays in the command operating mode until a subsequent OPERATION command or a state altering of the EN1 pin change rail1 to another mode.

Command	OPERATION							
Format	Unsigned binary							
BIT	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r	r
Function	OPERATION_MODE							

Bits	Bit Name	Description
7:0	OPERATION_MODE	Set the operation mode for rail1. 7’b00xxxxxx: High-Z off 7’b01xxxxxx: Soft off 7’b1000xxxx:Normal on 7’b1001xxxx: Margin low 7’b1010xxxx: Margin high “x” means don't care.

MFR_CLK_MASTER (02h)

The MFR_CLK_MASTER command is used to set the sync clock input/output mode and power on/off sequence syncing for both rails when multiple mEZD81260A is applied in the same system.

Command	MFR_CLK_MASTER							
Format	Unsigned binary							
BIT	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	X			

Bits	Bit Name	Description
7:3	RESERVED	Unused. X indicates writes are ignored and always read as 0.
2	CLK_IN_OUT_SEL	CLK pin input or output type selection bit. When power on/off sync function is not used, set this bit to 0 and pull CLK to 3.3V through a 4.99KΩ resistor. 1'b0: CLK pin is the input pin. It will input 200KHz clock at power on/off sync mode. The mEZD81260A works as a slave. 1'b1: CLK pin is the output pin. It outputs 200KHz sync clock at power on/off sync mode. The mEZD81260A works as a master.
1	SYNC_ON	Power on synchronous enabled bit. 1'b0: disable power on synchronous. The power on related timings follow internal clock. 1'b1: enable power on synchronous. The power on related timings follow 200KHz clock from CLK pin. If CLK pin is pulled high, the power on sequence follows internal clock.
0	SYNC_OFF	Power off synchronous enabled bit. 1'b0: disable power off synchronous. The power off related timings follow internal clock. 1'b1: enable power off synchronous. The power off related timings follow 200KHz clock from CLK pin. If CLK pin is pulled high, the power on sequence follows internal clock.

For standalone application, set MFR_CLK_MASTER (02h) = 0x00 and pull CLK pin high.

CLEAR_FAULTS (03h)

The CLEAR_FAULTS command is used to clear the system fault after system initialization ends. CLEAR_FAULTS is written only and there is no data byte for it. It is effective for both rails no matter the value of PAGE command. The faults include VIN UVLO, VIN OVP, OTP, output OVP, UVP, OCP-Total protections, PMBus communication faults and EEPROM faults. Once send a CLEAR_FAULTS, the faults listed above on both rails are cleared and the fault bits in register MFR_FAULTS (86h) and MFR_CML (87h) are all reset if the associate fault is removed.

STORE_USER_ALL (15h)

The STORE_USER_ALL command instructs the PMBus device to copy the page0 and page1 values in the operating memory to the matching locations in the EEPROM. Any items in operating memory that do not have matching locations in the EEPROM are ignored.

It is permitted to use this command while the device is outputting power.

This command is written only. There is no data byte for this command.

RESTORE_USER_ALL (16h)

The RESTORE_USER_ALL command instructs the PMBus device to copy the page0 and page1 value of the EEPROM to the matching locations in the operating memory. The values in the operating memory are overwritten by the value retrieved from the EEPROM. Any items in the EEPROM that do not have matching locations in the operating memory are ignored.

It is **NOT** permitted to use this command while the device is outputting power, or the command will be ignored.

This command is written only. There is no data byte for this command.

VOUT_COMMAND (21h)

The VOUT_COMMAND on page0 sets the rail1 nominal output voltage value in VID format.

Command	VOUT_COMMAND															
Format	VID															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	X	X	VOUT_VID									

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates writes are ignored and always read as 0.
9:0	VOUT_VID	Set the Rail1 nominal output voltage level in VID format. 5mV/LSB.

VOUT_TRIM (22h)

The VOUT_TRIM command on page0 is used to apply an offset value to the rail1 reference voltage (VREF). It is generally used by the end users to trim the output voltage at the time the PMBus device is assembled into the end user's system. It also can be used to fine tune the output voltage when the designed VREF is output 5mV step.

Command	VOUT_TRIM															
Format	Signed binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	X	X	X	X	X	X	X	X	VREF_TRIM			

Bits	Bit Name	Description
15:4	RESERVED	Unused. X indicates writes are ignored and always read as 0.
3:0	VREF_TRIM	Add a fixed offset over the VREF of rail1. 3.13mV/LSB. It is in twos compliment format. Bit[3] is the sign bit. The voltage list below shows the direct value and real world value. 4'b0000: 0mV 4'b0001: +3.13mV 4'b0111: +21.91mV 4'b1000: 0mV 4'b1001: -21.91mV 4'b1111: -3.13mV

VOUT_MARGIN_HIGH (25h)

The VOUT_MARGIN_HIGH command sets the margin high voltage level to which the output is to be changed when the OPERATION command is set to "Margin High".

Command	VOUT_MARGIN_HIGH															
Format	VID															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	X	X	VOUT_MARGIN_HIGH									

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates writes are ignored and always read as 0.
9:0	VOUT_MARGIN_HIGH	Set the Rail1 margin high state output voltage level. 5mV/LSB.

VOUT_MARGIN_LOW (26h)

The VOUT_MARGIN_LOW command sets the margin low voltage level to which the output is to be changed when the OPERATION command is set to “Margin Low”.

Command	VOUT_MARGIN_LOW															
Format	VID															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	X	X	VOUT_MARGIN_LOW									

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates writes are ignored and always read as 0.
9:0	VOUT_MARGIN_LOW	Set the Rail1 margin low state output voltage level. 5mV/LSB.

VOUT_SCALE_LOOP (29h)

The VOUT_SCALE_LOOP command on page0 sets the rail1 output voltage to reference voltage dividing ratio.

Command	VOUT_SCALE_LOOP															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	X	X	X	X	VOUT_SCALE_LOOP							

Bits	Bit Name	Description
15:8	RESERVED	Unused. X indicates writes are ignored and always read as 0.
7:0	VOUT_SCALE_LOOP	Set the rail1 output voltage to reference voltage VREF dividing ratio with the following equation. VREF ranges from 0.245-1.52V. $VOUT\_SCALE\_LOOP = 128 \times \frac{V_{REF}}{V_{OUT}}$

For example, to support 5V output voltage, select VREF=0.82V, then VOUT_SCALE_LOOP (29h) = 0x0015.

FREQUENCY_SWITCH (33h)

The FREQUENCY_SWITCH command on page0 is used to set the switching frequency for rail1. The switching frequency range is from 200KHz to 2MHz, with 10KHz per step.

Command	FREQUNCY_SWITCH															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	X	X	X	X	SWITCH_FREQUENCY							

Bits	Bit Name	Description
15:8	RESERVED	Unused. X indicates writes are ignored and always read as 0.
7:0	SWITCH_FREQUENCY	Set the rail1 switching frequency from 200-2000KHz. 10KHz/LSB.

VIN_ON (35h)

The VIN_ON command is used to set the V_{IN} UVLO rising threshold.

Command	VIN_ON															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	X	X	X	X	X	VIN_ON						

Bits	Bit Name	Description
15:7	RESERVED	Unused. X indicates writes are ignored and always read as 0.
6:0	VIN_ON	Set the V_{IN} UVLO rising threshold. 0.25V/LSB.

For example, when the V_{IN} UVLO rising threshold is 8V, then set VIN_ON (35h)=0x0020.

VIN_OFF (36h)

The VIN_OFF command is used to set the V_{IN} UVLO falling threshold.

Command	VIN_OFF															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	X	X	X	X	X	VIN_OFF						

Bits	Bit Name	Description
15:7	RESERVED	Unused. X indicates writes are ignored and always read as 0.
6:0	VIN_OFF	Set the V_{IN} UVLO falling threshold. 0.25V/LSB.

For example, when the Vin UVLO falling threshold is 7V, then set VIN_OFF (36h)=0x001C.

VIN_OV_FAULT_LIMIT (55h)

The VIN_OV_FAULT_LIMIT command is used to set the V_{IN} OVP threshold. Once the input voltage exceeds the VIN_OV threshold, the power regulation system will latch down. Require OPERATION command, EN toggling or VIN power cycle to restart the power system.

Command	VIN_OV_FAULT_LIMIT															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	X	X	X	X	X	VIN_OV						

Bits	Bit Name	Description
15:7	RESERVED	Unused. X indicates writes are ignored and always read as 0.
6:0	VIN_OV	Set the V_{IN} OVP latches off threshold. 0.25V/LSB.

For example, when the Vin OVP threshold is 16V, then set VIN_OV_FAULT_LIMIT (55h)=0x0040.

TON_DELAY (60h)

The TON_DELAY command on page0 is used to set the rail1 power on delay time.

Command	TON_DELAY															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	TON_DELAY															

Bits	Bit Name	Description
15:0	TON_DELAY	Set the rail1 power on delay time. The power on delay time starts when the system initialization is completed. When the Ton delay time is over, rail1 begins soft-starts. 100us/LSB.

For example, to get 10ms power on delay time, set TON_DELAY (60h)=0x0064.

TON_RISE (61h)

The TON_RISE command on page0 is used to set the rail1 VREF soft-start slew rate. Figure-8 shows the definition of sub-registers in TON_RISE.

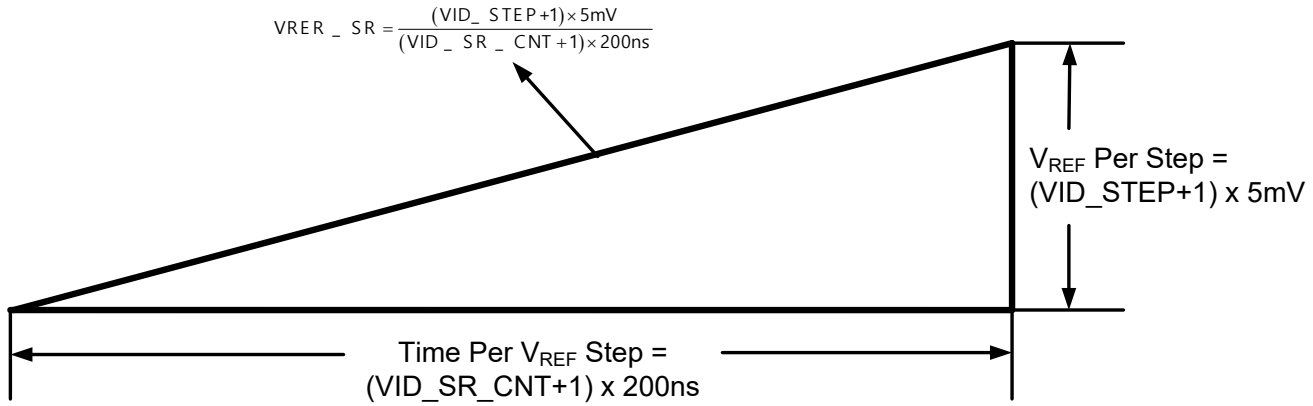


Figure 8: Soft-Start Slew Rate Definition

The output voltage soft-start slew rate can be calculated with Equation (6):

$$VOUT\_SR = \frac{(VID\_STEP+1)\times 5mV}{(VID\_SR\_CNT+1)\times 200ns}\times\frac{1}{K_{R1}} \quad (6)$$

Where,

K_{R1} is the rail1 output divider ratio.

Command	TON_RISE															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	VID_STEP		VID_SR_CNT										

Bits	Bit Name	Description
15:13	RESERVED	Unused. X indicates writes are ignored and always read as 0.
12:11	VID_STEP	At soft-start, VREF is rising step by step. VID_STEP sets the VREF amplitude for each step in VID format. The VREF per step can be calculated with: (VID_STEP+1)*5mV. 5mV/LSB.
10:0	VID_SR_CNT	Set the duration time for each VREF step. The time can be calculated with equation: (SS_SR_CNT+1)*200ns. 200ns/LSB.

For example, if VID_STEP= 2'b00, DVID_SR_CNT=0, the soft start slew rate is 25mV/us.

TOFF_DELAY (64h)

The TOFF_DELAY command on page0 is used to set the rail1 power off delay time. Power off delay time is only effective at OPERATION command soft-off.

Command	TOFF_DELAY															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	TOFF_DELAY															

Bits	Bit Name	Description
15:0	TOFF_DELAY	Set the rail1 power off delay time at OPERATION command soft-off. 100us/LSB.

TOFF_FALL (65h)

This TOFF_FALL command is used to set the DVID and soft-shutdown slew rate. The sub-register definition is same as Figure-8. The slew rate can be calculated with equation (6)

Command	TOFF_FALL															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	VID_STEP		VID_SR_CNT										

Bits	Bit Name	Description
15:13	RESERVED	Unused. X indicates writes are ignored and always read as 0.
12:11	VID_STEP	At dynamic VID transition and soft off, VREF is changing step by step. VID_STEP sets the VREF amplitude for each step in VID format. The VREF per step can be calculated with: (VID_STEP+1)*5mV. 5mV/LSB.
10:0	VID_SR_CNT	Set the duration time for each VREF step. The time can be calculated with equation: (VID_SR_CNT+1)*200ns. 200ns/LSB.

MFR_FAULTS (86h)

The MFR_FAULTS command is used to return the VR operation faults at present power cycle. It is a read only command. Each fault bit represents a fault type. The fault bits are all in latch mode. Once it is set, require a CLEAR_FAULT command, EN or VIN power recycle to reset it.

Command	MFR_FAULTS															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	X	X	X									

Bits	Bit Name	Description
15:9	RESERVED	Unused. X indicates writes are ignored and always read as 0.
8	IOUT_OC _R2	Rail2 OCP-Total fault indication bit. 1'b0: no OCP-Total fault on rail2; 1'b1: OCP-Total fault has occurred on rail2.
7	IOUT_OC _R1	Rail1 OCP-Total fault indication bit. 1'b0: no OCP-Total fault on rail1; 1'b1: OCP-Total fault has occurred on rail1.
6	VOUT_UV _R2	Rail2 V_{OUT} UV fault indication bit. It is set when rail2 V_{OUT} UVP blanking time ends and V_{OUT} UV still exists. 1'b0: no V_{OUT} UV fault on rail2; 1'b1: V_{OUT} UV fault has occurred on rail2.
5	VOUT_UV _R1	Rail1 V_{OUT} UV fault indication bit. It is set when rail1 V_{OUT} UVP blanking time ends and V_{OUT} UV still exists. 1'b0: no V_{OUT} UV fault on rail1; 1'b1: V_{OUT} UV fault has occurred on rail1.
4	VOUT_OV _R2	Rail2 V_{OUT} OV fault indication bit. It is set when rail2 V_{OUT} OVP blanking time ends and V_{OUT} OV still exists. 1'b0: no V_{OUT} OV fault on rail2; 1'b1: V_{OUT} OV fault has occurred on rail2.
3	VOUT_OV _R1	Rail1 V_{OUT} OV fault indication bit. It is set when rail1 V_{OUT} OVP blanking time ends and V_{OUT} OV still exists. 1'b0: no V_{OUT} OV fault on rail1; 1'b1: V_{OUT} OV fault has occurred on rail1.
2	OT_FLT	Over temperature fault indication bit. 1'b0: no OT fault has occurred; 1'b1: OT fault has occurred.
1	VIN_OV	V_{IN} OV fault indication bit. 1'b0: no V_{IN} OV fault has occurred; 1'b1: V_{IN} OV fault has occurred.
0	VIN_UV	V_{IN} UV fault indication bit. 1'b0: no V_{IN} UV fault has occurred; 1'b1: V_{IN} UV fault has occurred.

For example, if MFR_FAULTS = 0002H, it means V_{IN} OV fault has occurred.

MFR_CML (87h)

The MFR_CML command returns the PMBus command and data communication fault and EEPROM fault status. It is also used to lively indicate the present PMBus command is for EEPROM or operating memory. It is a read only command.

Command	MFR_CML							
Format	Unsigned binary							
BIT	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	X	X	PAGE	

Bits	Bit Name	Description
7	CMD_FLT	Indicate invalid PMBus command; 1'b0: no invalid PMBus command has been received; 1'b1: an invalid PMBus command has been received.
6	DATA_FLT	Indicate invalid PMBus data; 1'b0: no invalid PMBus data has been received; 1'b1: an invalid PMBus data has been received.
5, 3:2	RESERVED	Unused. X indicates writes are ignored and always read as 0.
4	EEPROM_FLT	EEPROM fault indication. 1'b0: no EEPROM fault has occurred; 1'b1: an EEPROM fault has occurred.
1	PMBUS_OTHER	Other PMBus communication faults indication 1'b0: no other PMBus communication faults; 1'b1: a PMBus communication fault besides invalid command and data has occurred.
0	EEPROM_WR_IND	1'b0: the operation is not for EEPROM (idle or for operating memory) 1'b1: the operation is for EEPROM.

The fault bits are all in latch mode. Once it is set, require a CLEAR_FAULT (03) command to reset it. The bit 0 is not a fault bit. It is a live mode indication bit.

READ_VIN (88h)

The READ_VIN command is used to monitor the input voltage in direct format.

Command	READ_VIN															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	X	X	X	X	X	READ_VIN						

Bits	Bit Name	Description
15:7	RESERVED	Unused. X indicates writes are ignored and always read as 0.
6:0	READ_VIN	Report input voltage in direct format. 0.25V/LSB. For example, if READ_VIN=0x0030, it means the sensed input voltage is 12V.

READ_VOUT (8Bh)

The READ_VOUT command on page0 is used to return the ADC sensed VDIFF voltage on rail1. Then the PMBus reported output voltage can be calculated with Equation (7):

$$VOUT\_REPORT = \frac{3.13\ (mV) \times READ\_VOUT}{K_{R1}} \quad (7)$$

Command	READ_VOUT															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	X	X	READ_VOUT									

Bits	Bit Name	Description
15:7	RESERVED	Unused. X indicates writes are ignored and always read as 0.
6:0	READ_VOUT	Return the ADC sensed voltage on rail1 VDIFF1 pin. 3.13mV/LSB.

READ_IOUT (8Ch)

The READ_IOUT command is used to monitor the rail1 total average load current in direct format.

Command	READ_IOUT															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	X	X	X	X	READ_IOUT							

Bits	Bit Name	Description
15:8	RESERVED	Unused. X indicates writes are ignored and always read as 0.
7:0	READ_IOUT	Monitor the rail1 total average load current in direct format. 0.5A/LSB. For example, when READ_IOUT=0x0020, the rail1 load current is 16A.

READ_TEMPERATURE (8Dh)

The READ_TEMPERATURE command is used to monitor the power stage temperature. The mEZD81260A monitors power stage temperature by sensing the voltage on VTEMP pin, and convert it to direct format internal the device. To convert VTEMP voltage to temperature, set the temperature sense gain and offset with command MFR_TEMP_CAL (D2h).

Command	READ_TEMPERATURE															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	X	X	X	X	READ_TEMPERATURE							

Bits	Bit Name	Description
15:8	RESERVED	Unused. X indicates writes are ignored and always read as 0.
7:0	READ_TEMPERATURE	Monitor the temperature of the power stage. 1℃/LSB.

MFR_CS (8Fh)

The MFR_CS command on page0 is used to monitor the phase1 average inductor current.

Command	MFR_CS							
Format	Unsigned binary							
BIT	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	READ_IPHASE						

Bits	Bit Name	Description
7	RESERVED	Unused. X indicates writes are ignored and always read as 0.
6:0	READ_IPHASE	Return the sensed phase1 average current. 0.5A/LSB.

MFR_VR_CONFIG (D0h)

The MFR_VR_CONFIG command is used to configure the basic functions of the mEZD81260A.

Command	MFR_VR_CONFIG															
Format	Binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function																

Bits	Bit Name	Description
15	DRL_ITLV_EN	Phase1 and Phase2 interleaving enable bit at dual rail mode. It is only effective at CCM mode, both rails are set with same switching frequency and frequency loop is enabled. Besides these conditions, the interleaving function at dual rail is ignored even though DRL_ITLV_EN=1. 1'b0: dual rail interleaving is disabled; 1'b1: dual rail interleaving is enabled.
14	OSR_EN	Over shot reduction (OSR) function enable bit for both rails. When OSR is enabled, the mEZD81260A will turn off high side MOSFET once the sense VOUT exceeds a certain threshold. It is generally used at multi-phase applications. 1'b0: disable OSR function 1'b1: enable OSR function.
13	VIN_CAL_TON_EN	Update PWM on time with real time input voltage enable bit. Once enable this function, T_{ON} changes with V_{IN} and to keep the switching frequency constant with different VIN. 1'b0: T_{ON} will not update with real time V_{IN}; 1'b1: T_{ON} will update with real time V_{IN};
12	DR_DP_SEL	The mEZD81260A dual rail and dual phase mode selection bit. 1'b0: dual rail mode; 1'b1: dual phase mode.
11	IBALANCE_EN	Dual phase current balance function enable bit. It is in-effective at dual rail mode. 1'b0: disable current balance at dual phase mode; 1'b1: enable current balance at dual phase mode.
10	DCLOOP_DCM_EN_R2	Rail2 DC loop enable bit at DCM. 1'b0: disable DC loop at DCM for rail2; 1'b1: enable DC loop at DCM for rail2, only effective when command D0h, bit8=1.
9	DCLOOP_DCM_EN_R1	Rail1 DC loop enable bit at DCM. 1'b0: disable DC loop at DCM for rail1; 1'b1: enable DC loop at DCM for rail1, only effective when command D0h, bit7=1.

8	DCLOOP_EN_R2	Rail2 DC loop global enable bit. It is active both at DCM and CCM mode. 1'b0: disable DC loop for rail2; 1'b1: enable DC loop for rail2.
7	DCLOOP_EN_R1	Rail1 DC loop global enable bit. It is active both at DCM and CCM mode. 1'b0: disable DC loop for rail1; 1'b1: enable DC loop for rail1.
6	TEST_MODE1	A test mode bit. Always set it to 0 at normal operation.
5:4	TON_OS_DCM_R2	Set the PWM on time offset at DCM for rail2. 2'b00, 2'b01: T_{ON} keeps same as CCM. 2'b10: T_{ON} is reduced by a quarter to reduce the output voltage ripple at DCM; 2'b11: T_{ON} is added by a quarter to reduce the switching frequency, thus to improve the efficiency at DCM;
3:2	TON_OS_DCM_R1	Set the PWM on time offset at DCM for rail1. 2'b00, 2'b01: T_{ON} keeps same as CCM. 2'b10: T_{ON} is reduced by a quarter to reduce the output voltage ripple at DCM; 2'b11: T_{ON} is added by a quarter to reduce the switching frequency, thus to improve the efficiency at DCM;
1	FS_LOOP_EN	Switching frequency loop enable bit. Frequency loop is used to keep the switching frequency flat and equals to the setting value. It is active for both rails. 1'b0: disable frequency loop; 1'b1: enable frequency loop.
0	ULTRASONIC_EN	Ultra-sonic mode enable bit at DCM mode. It is active for both rails. 1'b0: disable ultra-sonic mode; 1'b1: enable ultra-sonic mode. The frequency keeps above 25kHz at DCM when set it to 1.

MFR_VIN_SCALE_LOOP (D4h)

The MFR_VIN_SCALE_LOOP command is used to program the input voltage sense divider ratio into the mEZD81260A. The mEZD81260A senses the voltage on VINSENS pin and convert it to input voltage. The sensed V_{IN} is used to calculate TON together with the value in register MFR_VIN_SCALE_LOOP (D4h).

Command	MFR_VIN_SCALE_LOOP							
Format	Unsigned binary							
BIT	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	VIN_SCALE_LOOP							

Bits	Bit Name	Description
7:0	VIN_SCALE_LOOP	Set the input voltage sense divider ratio with the following equation: $MFR\_VIN\_SCALE\_LOOP = 2^{10} \times \frac{R_{IN2}}{R_{IN1} + R_{IN2}}$

For example, select RIN1=54.9K, and RIN2=4.99K, then set MFR_VIN_SCALE_LOOP (D4h) = 0x55.

MFR_OCP_TOTAL_SET (D6h)

The MFR_OCP_TOTAL_SET command on page0 is used to set the rail1 total current protection level, protection mode and OCP blanking time. OCP_Total is a time based over current protection. It should be tripped when the sensed average output current exceeds the threshold for a period of time. This period of time is referred as OCP blanking time. The OCP_Total can be programmed to No Action, Hiccup, Retry 6-Time and Latch-Off mode via PMBus.

Command	MFR_OCP_TOTAL_SET															
Format	Binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	MODE			OCP_BLANKING_TIME				OCP_LIMIT_LSB					

Bits	Bit Name	Description
15:13	RESERVED	Unused. X indicates writes are ignored and always read as 0.
12:11	MODE	Set OCP-Total protection action mode. There are four modes available. 2'b00: No Action; 2'b01: Latch-Off; 2'b10: Hiccup; 2'b11: Retry 6-Time.
10	OCP_LIMIT_HSB	Set the OCP-Total threshold together with OCP_LIMIT_LSB. Bit10 is the highest bit and acts as sixth bit for entire OCP-LIMIT setting.
9:6	OCP_BLANKING_TIME	Set OCP-Total protection blanking time. An OCP-Total fault is occurred if the current exceeds the OCP-TOTAL threshold for an OCP blanking time 100us/LSB.
5:0	OCP_LIMIT_LSB	Set the OCP-Total threshold together with OCP_LIMIT_HSB. OCP_LIMIT_LSB is the lower 5 bits. The OCP-Total threshold ranges from 0 to 127A. 1A/LSB.

For example, when set MFR_OCP_TOTAL_SET=0x0965, the OCP_total current limit level is 30A, OCP_total protection mode is latch off with 500us OCP blanking time.

MFR_OVP_SET (D7h)

The MFR_OVP_SET command on page0 is used to set the rail1 output over voltage protection level, mode and blanking time.

Command	MFR_OVP_SET															
Format	Binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X		MODE		OVP_BLANKING_TIME`									

Bits	Bit Name	Description
15:13	RESERVED	Unused. X indicates writes are ignored and always read as 0.
12	VFB+_WINDOW_EN	VFB+ Window enable bit. VFB+ window is a VFB+25mV threshold. It is used for output overshot reduction and DC loop hold function. 1'b0: VFB+ Window is disabled; 1'b1: VFB+ Window is enabled.
11:10	OVP1_MODE	Set V_{OUT} OVP1 protection mode. There are four modes available. 2'b00: No Action; 2'b01: Latch-Off; 2'b10: Hiccup; 2'b11: Retry 6-Time.
9:4	OVP1_BLANKING_TIME	Set V_{OUT} OVP1 blanking time. An OVP fault is occurred if the sensed VDIFF exceeds the OVP1 threshold for an OVP blanking time 100ns/LSB.
3:2	OVP2_LIMIT	Set OVP2 threshold. OVP2 is a regulation type threshold. If the voltage on VDIFF exceeds the OVP2 threshold, the MEZD81260A turns on low side MOSFET to discharge output voltage below OVP2 threshold. 2'b00: VREF+100mV; 2'b01: VREF+200mV; 2'b10: VREF+300mV; 2'b11: VREF+400mV
1:0	OVP1_LIMIT	Set OVP1 threshold. OVP1 is a protection type threshold. If the voltage on VDIFF exceeds the OVP1 threshold, the MEZD81260A turns on low side MOSFET to discharge output voltage and takes action to Latch-Off, Hiccup or Retry 6-Time as programmed by OVP1_MODE. At No Action mode, the MEZD81260A keeps switching and the OVP fault bit in register MFR_FALUTS (86h) will not assert. Always design OVP1_LIMIT higher than OVP2_LIMIT. 2'b00: VREF+100mV; 2'b01: VREF+200mV; 2'b10: VREF+300mV; 2'b11: VREF+400mV.

For example, when set MFR_OVP_SET=0x1456, the OVP setting of rail1 is: Disable VFB+ window; OVP2 threshold is VREF+200mV; OVP1 threshold is VREF+300mV and the rail1 latches down once VDIFF1 exceeds OVP1 threshold for 500ns.

MFR_UVP_SET (D8h)

The MFR_UVP_SET command on page0 is used to set the rail1 under voltage protection mode, level and delay time.

Command	MFR_UVP_SET															
Format	Binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X													

Bits	Bit Name	Description
15:11	RESERVED	Unused. X indicates writes are ignored and always read as 0.
10	VFB-_WINDOW_EN	VFB- Window enable bit. VFB- window is a VFB-25mV threshold. It is can be used to expedite load transient response at APM mode. 1'b0: VFB- Window is disabled; 1'b1: VFB- Window is enabled.
9:8	UVP_MODE	Set V_{OUT} UVP protection action mode. There are four modes available. 2'b00: No Action; 2'b01: Latch-Off; 2'b10: Hiccup; 2'b11: Retry 6-Time.
7:2	UVP_BLANKING_TIME	Set V_{OUT} UVP blanking time. An UVP fault is occurred if the sensed VDIFF falls below the UVP threshold for an UVP blanking time 100ns/LSB.
1:0	UVP_LIMIT	Set UVP threshold. If the voltage on VDIFF falls below the UVP threshold, the mEZD81260A takes no action or acts to Latch-Off, Hiccup or Retry 6-Time as programmed by UVP_MODE. At No Action mode, the mEZD81260A keeps switching and the UVP fault bit in register MFR_FALUTS (86h) will not assert. 2'b00: VREF+100mV; 2'b01: VREF+200mV; 2'b10: VREF+300mV; 2'b11: VREF+400mV.

MFR_OTP_SET (D9h)

The MFR_OTP_SET command is used to set the over temperature protection threshold and retry hysteresis.

Command	MFR_OTP_SET															
Format	Binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	OTP_HYS						OTP_LIMIE							

Bits	Bit Name	Description
15:14	RESERVED	Unused. X indicates writes are ignored and always read as 0.
13:8	OTP_HYS	Set the OTP retry hysteresis. When the OTP action mode in command MFR_PRT_CONFIG (DCh) is programmed to Retry mode, the mEZD81260A tries to restart when the sensed temperature on VTEMP pin falls below OTP_LIMIT-OTP_HYS. 1℃/LSB.
7:0	OTP_LIMIT	Set the over temperature threshold. When sense temperature on VTEMP pin exceeds OTP_LIMIT, the mEZD81260A shuts off both VOUT immediately. 1℃/LSB.

MFR_OCP_PHASE_SET (DAh)

The MFR_OCP_PHASE_SET command on page0 is used to set the phase1 OCP-Phase current limit. OCP-Phase is a single phase valley current limitation threshold. The mEZD81260A monitors phase current cycle-by-cycle. When the phase current exceeds the OCP-Phase threshold at PWM off time, PWM keeps low to discharge inductor current below the set threshold.

Command	MFR_OCP_PHASE_SET															
Format	Binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	X	X	X	X	OCP_PHASE_LIMIT							

Bits	Bit Name	Description
15:8	RESERVED	Unused. X indicates writes are ignored and always read as 0.
7:0	OCP_PHASE_LIMIT	Set the per phase valley current limit threshold.

The OCP valley current is calculate with equation (8):

$$OCP\_PHASE\_LIMIT = 100 \times I_{OC\_VALLEY} \times K_{CS} \times R_{CS} + 26 \quad (8)$$

where:

I_{OC_VALLEY} is the per phase valley current limit, in A;

K_{CS} is the current sense gain of Intelli-Phase, in A/A;

R_{CS} is the CS resistor internal mEZD81260A, in Ω. It is typically 1.4KΩ;

For example, to get 21A OCP-Phase valley current limit, set MFR_OCP_LIMIT=0x0036.

MFR_PRT_RETRYTIME (DBh)

The MFR_PRT_RETRYTIME command on page0 is used to set protections retry delay time for both rails. It is effective at Hiccup and Retry 6-Time protection modes.

Command	MFR_PRT_RETRYTIME							
Format	Unsigned binary							
BIT	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	PRT_RETRY_TIME			

Bits	Bit Name	Description
7:4	RESERVED	Unused. X indicates writes are ignored and always read as 0.
3:0	PRT_RETRY_TIME	Set the retry delay time at Hiccup and Retry 6-Time protection modes. 800us/LSB.

The entire retry delay time from the previous fault shutdown to the next restarting can be calculated with Equation (9):

$$T_{PRT\_RETRY} = PRT\_RETRY\_TIME \times 800\mu s + TON\_DELAY + 700\mu s \quad (9)$$

where,

TON_DELAY is the power on delay time programmed by command TON_DELAY (60h), in us.

MFR_PRT_CONFIG (DCh)

The MFR_PRT_CONFIG command is used to set protections behaviors.

Command	MFR_PRT_CONFIG							
Format	Unsigned binary							
BIT	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X					

Bits	Bit Name	Description
7:5, 2	RESERVED	Unused. X indicates writes are ignored and always read as 0.
4	FLT_ REC_EEPROM	Record the faults bits in register MFR_FAULTS (86h) to EEPROM enable bit. The mEZD81260A can store the fault type into EEPROM automatically once a fault lists in MFR_FAULTS has occurred. The fault type will be loaded to the read only register MFR_FAULT_RECORD (F8h) at the next power on cycle. It is very useful at the debugging stage. To save the EEPROM life, do not enable this function at production stage. 1'b0: disable fault type storing into EEPROM; 1'b1: enable fault type storing into EEPROM
3	FAULT_DR_SDN	A fault on single rail will shutdown both rails enable bit. 1'b0: the fault action of both rails is independent; 1'b1: enable fault shuts down both rails. When a fault happens on any rail, the other rail will response to this fault with the same protection mode as the fault rail.
1	TEST_MODE2	TEST_MODE2 **disable** bit. Always set it to **1** at normal operation.
0	OTP_MODE	Set the over temperature protection mode. 1'b0: Latch-Off mode; 1'b1: Retry mode.

MFR_BLANK_TIME (E1h)

The MFR_BLANK_TIME command is used to set the minimum time between two neighbor PWMs at dual phase operation. Blanking time makes the system stable by limiting the multi-phase maximum frequency at the transient conditions. Recommend the blanking time >60ns at dual phase operation. Blanking time is also used to set the slope compensation voltage initiating point (see Register Map/ MFR_SLOPE_SR_PS0 (E2h)).

Command	MFR_BLANK_TIME							
Format	Direct							
BIT	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	BLANKING_TIME					

Bits	Bit Name	Description
7:6	RESERVED	Unused. X indicates writes are ignored and always read as 0.
5:0	BLANKING_TIME	Set the minimum time between two neighbor phases at dual phase operation. And set the slope compensation initiate point. 5ns/LSB.

MFR_SLOPE_SR_PS0 (E2h)

Slope compensation is used to provide enough noise immunity for PWM generation and make the PWM switches stable on the mEZD81260A. The slope compensation is generated by a PMBus programmable current source and a PMBus programmable capacitor.

The mEZD81260A provides slope voltage programming command for each power state. The MFR_SLOPE_SR_PS0 command on page0 is used to set the slew rate of slope compensation for rail1 at PS0 (2-phase CCM).

Command	MFR_SLOPE_SR_PS0															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	X	X	X	CAP			CURRENT_SOURCE					

Bits	Bit Name	Description
15:9	RESERVED	Unused. X indicates writes are ignored and always read as 0.
8:6	CAP	Set the capacitance for slope compensation at 2-phase CCM. The capacitance can be calculated with: $(8-CAP)\times 3.7pF$
5:0	CURRENT_SOURCE	Set the current source value for slope compensation at 2-phase CCM. The current source can be calculated with: $CURRENT\_SOURCE\times 0.25\mu A$

The slope slew rate of 2-phase CCM (PS0) is calculated with equation (10):

$$SLOPE\_SR_{@PS0} = 16892\times\frac{CURRENT\_SOURCE}{(8-CAP)} \quad (10)$$

where,

The slope voltage slew rate SLOPE_SR is in V/s.

Figure-9 shows a slope voltage curve at 2-phase CCM.

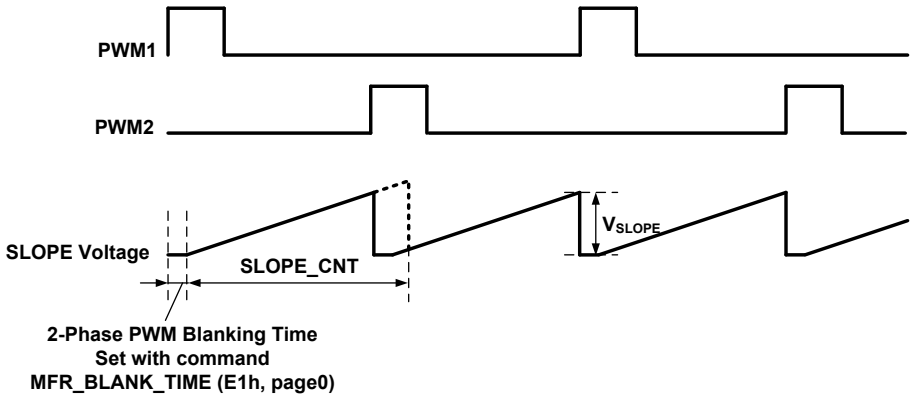


Figure-9 Slope voltage at 2-phase CCM power sate

The slope voltage amplitude (V_{SLOPE}) can be calculated with equation 11.

$$V_{SLOPE} = SLOPE\_SR_{@PS0}\times\left(\frac{T_{SW}}{2}-t_{BLANK}\right) \quad (11)$$

where,

T_{SW} is the single phase switching period set with command FREQUENCY_SWITCH (33h), in s;

t_{BLANK} is the PWM blanking time set with command MFR_BLANK_TIME (E1h), in s.

In general design guideline, the slope voltage amplitude V_{SLOPE} of 20mV to 30mV is used to cover all potential Ton, L and Cout variation. Lower slope voltage tends to faster load transient response, while higher slope voltage leads to better noise immunity (less PWM jittering).

MFR_SLOPE_CNT_PS0 (E3h)

The MFR_SLOPE_CNT_PS0 command on page0 is used to set the slope voltage clamp time. The clamp time is used to limit the slope voltage when switching off-time is too long, i.e. DCM operation or output load release transient. It should cover the regular PWM switching off-time. The slope voltage is clamped once the clamp timer expires, which means no slope compensation any more. To give enough time margins for slope compensation, recommend to design slope clamp timer with the 130% of switching off-time as shown in equation (12).

$$t_{SLOPE\_CLAMP} = 1.3 \times \left(\frac{T_{SW}}{2} - t_{BLANK} \right) \quad (12)$$

Where,

t_{SLOPE_CLAMP} is the slope clamping timer, in s;

T_{SW} is the single phase switching period, in s;

t_{BLANK} is the PWM blanking time set with command MFR_BLANK_TIME (E1h), in s.

Command	MFR_SLOPE_CNT_PS0							
Format	Direct							
BIT	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	SLOPE_CNT							

Bits	Bit Name	Description
7:0	SLOPE_CNT	Set the slope clamp timer for PS2. 5ns/LSB.

MFR_SLOPE_SR_PS1 (E4h)

The MFR_SLOPE_SR_PS1 command on page0 is used to set the slew rate of slope compensation for rail1 at PS1 (1-phase CCM).

Command	MFR_SLOPE_SR_PS1							
Format	Direct							
BIT	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	CURRENT_SOURCE					

Bits	Bit Name	Description
7:6	RESERVED	Unused. X indicates writes are ignored and always read as 0.
7:0	CURRENT_SOURCE	Set the current source value for slope compensation at PS1. The current source can be calculated with: $CURRENT\_SOURCE \times 0.25\mu A$

The capacitance for slope compensation is 29.6pF. So the slope voltage (VSLOPE) for 1-phase CCM can be calculated with equation (13).

$$V_{SLOPE} = SLOPE\_SR_{@PS1} \times (T_{SW} - t_{BLANK}) = 2133 \times CURRENT\_SOURCE \times (T_{SW} - t_{BLANK}) \quad (13)$$

where,

The slope voltage slew rate SLOPE_SR is in V/s

T_{SW} is the single phase switching period set with command FREQUENCY_SWITCH (33h), in s;

t_{BLANK} is the PWM blanking time set with command MFR_BLANK_TIME (E1h), in s.

MFR_SLOPE_CNT_PS1 (E5h)

The MFR_SLOPE_CNT_PS1 command on page0 is used to set the slope voltage clamp time at PS1 (1-phase CCM).

Command	MFR_SLOPE_CNT_PS1															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	X	X	SLOPE_CNT									

Bits	Bit Name	Description
15:9	RESERVED	Unused. X indicates writes are ignored and always read as 0.
8:6	SLOPE_CNT	Set the slope clamp timer for PS1. 5ns/LSB.

The slope clamp time for PS1 can be calculated with equation (14).

$$t_{SLOPE\_CLAMP@PS1} = 1.3 \times (T_{SW} - t_{BLANK}) \quad (14)$$

MFR_SLOPE_SR_PS2 (E6h)

The MFR_SLOPE_SR_PS2 command on page0 is used to set the slew rate of slope compensation for rail1 at PS2 (1-phase DCM). The slope capacitance is fixed with 29.6pF.

Command	MFR_SLOPE_SR_PS2							
Format	Direct							
BIT	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	CURRENT_SOURCE					

Bits	Bit Name	Description
7:6	RESERVED	Unused. X indicates writes are ignored and always read as 0.
5:0	CURRENT_SOURCE	Set the current source value for slope voltage generation at PS2. The current source can be calculated with: $CURRENT\_SOURCE \times 0.25\mu A$

MFR_SLOPE_CNT_PS2 (E7h)

The MFR_SLOPE_CNT_PS2 command on page0 is used to set the slope voltage clamp time at PS2 (1-phase DCM). At 1-phase DCM, the off-time is increasing to reduce switching frequency as load current reducing. The slope voltage clamp time should be long enough to avoid the period of SW node freewheeling when the ZCD (Zero current detection) turns off the LS MOSFET to transit the SW node to Hi-Z, as shown in the Figure-10.

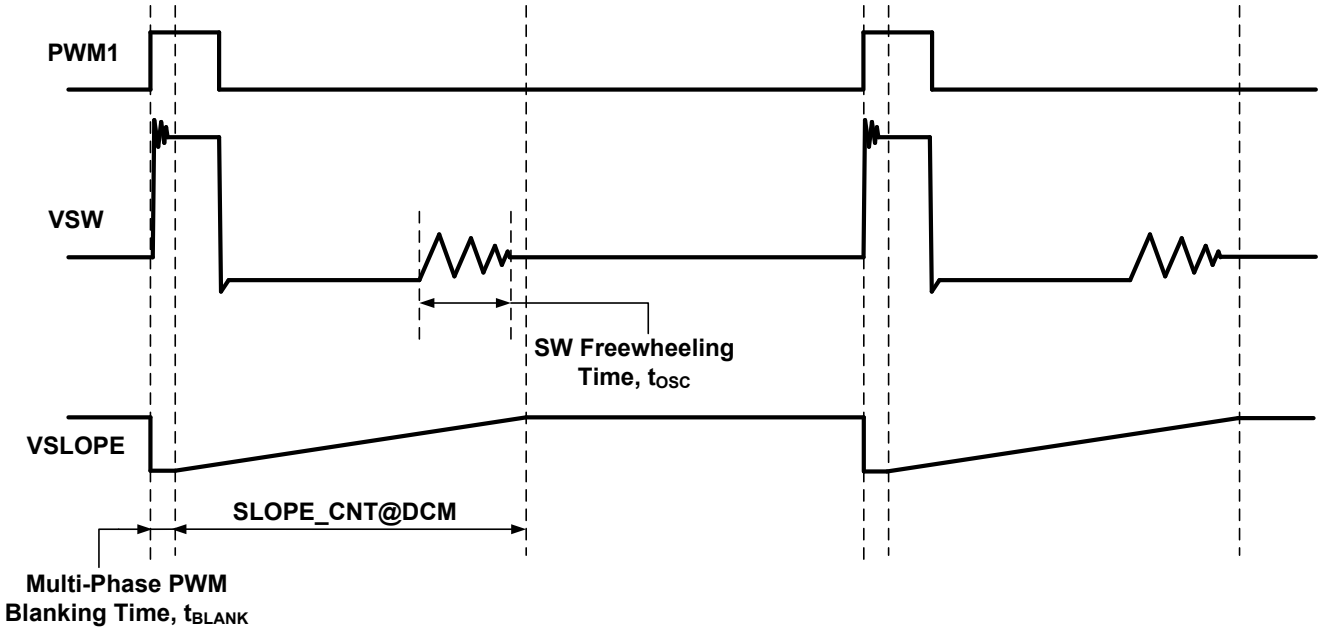


Figure-10 Slope voltage compensation at DCM

In general guideline, Recommend to use the equation (15) shown below to design the slope clamp time for DCM operation.

$$t_{SLOPE\_CLAMP@DCM} = 1.1 \times \left(T_{SW} - t_{BLANK} + t_{SW\_OSC} \right) \quad (15)$$

where,

$t_{SLOPE\_CLAMT@DCM}$ is the slope clamp time at 1-phase DCM, in s;

T_{SW} is the single phase switching period set with command FREQUENCY_SWITCH (33h), in s;

t_{BLANK} is the PWM blanking time set with command MFR_BLANK_TIME (E1h), in s;

t_{SW_OSC} is the switch node freewheeling time, in s.

Command	MFR_SLOPE_CNT_PS2							
Format	Direct							
BIT	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	SLOPE_CNT					

Bits	Bit Name	Description
7:6	RESERVED	Unused. X indicates writes are ignored and always read as 0.
5:0	SLOPE_CNT	Set the slope clamp time for PS2. 80ns/LSB.

MFR_SLOPE_SR_F25K (EAh)

The MFR_SLOPE_SR_F25K command on page0 is used to set the slope compensation slew rate for rail1 at ultra-sonic mode. This slope compensation takes action before each PWM on pulse when the switching cycle is limited to 40us.The slope capacitance is fixed with 3.9pF.

Command	MFR_SLOPE_SR_PS1							
Format	Direct							
BIT	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	CURRENT_SOURCE					

Bits	Bit Name	Description
7:6	RESERVED	Unused. X indicates writes are ignored and always read as 0.
5:0	CURRENT_SOURCE	Set the current source value for slope voltage generation at ultra-sonic mode. The current source can be calculated with: $CURRENT\_SOURCE \times 0.25\mu A$

In general designs, set CURRENT_SOURCE=2 to make the PWM on pulse stable at ultra-sonic mode.

MFR_PS01_TRIM (EBh)

When DC loop is disabled, the actual V_{OUT} voltage with the MEZD81260A can be calculated with equation (16).

$$V_{OUT} = \frac{V_{REF} - V_{SLOPE}}{K_R} + \frac{\Delta V_{OUT}}{2} \quad (16)$$

where,

V_{REF} is the reference voltage, in V;

V_{SLOPE} is the slope voltage, in V;

ΔV_{OUT} is the output voltage ripple, in V;

K_R is the output voltage divider.

The mEZD81260A provides reference voltage trim (referred as V_{TRIM}) to make the actual output voltage close the design target without DC-loop calibriation. It is implanted by add a negative offset over reference voltage. In designs, design the V_{TRIM} equals to the voltage shift caused by V_{SLOPE} and output voltage ripple. At auto power mode, the reference voltage trim also makes the DC loop output constant between different power sate, thus improve the load transient response between different power state.

The MFR_ PS01_TRIM command on page0 is used to trim the output voltage at 2-phase CCM (PS0) and 1-phase CCM (PS1) of rail1.

Command	MFR_PS01_TRIM															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X		VTRIM_PS1						VTRIM_PS0					

Bits	Bit Name	Description
15:13	RESERVED	Unused. X indicates writes are ignored and always read as 0.
12	AUTO_VTRIM_EN	Power state automatic trim function enable bit at force power state mode. 1'b0: disable to trim reference voltage automatically for each power state. 1'b1: enable to trim reference voltage automatically for each power state.
11:6	VTRIM_PS1	Set the reference voltage trim for PS1. 1.37mV/LSB
5:0	VTRIM_PS0	Set the reference voltage trim for PS0. 1.37mV/LSB

MFR_PS2_TRIM (ECh)

The MFR_ PS2_TRIM command on page0 is used to trim the output voltage at 1-phase DCM (PS2)

Command	MFR_PS2_TRIM															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	X	X	X	X	X	X	X	VTRIM_PS2				

Bits	Bit Name	Description
15:5	RESERVED	Unused. X indicates writes are ignored and always read as 0.
4:0	VTRIM_PS2	Set the reference voltage trim for PS0. 1.37mV/LSB

MFR_ADDR_PMBUS (EDh)

The MFR_ ADDR_PMBUS command is used to set the PMBUS address.

Command	MFR_ADDR_PMBUS							
Format	Unsigned Binary							
BIT	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function		ADDR_MSB			ADDR_LSB			

Bits	Bit Name	Description
7	ADDR_CONFIG_MODE	Set the PMBus address 4LSB setting mode. 1’b0: set the PMBus 4LSB by ADDR pin voltage; 1’b1: set the PMBus 4LSB by register.
6:4	ADDR_MSB	Set the 3MSB of PMBus address. It ranges from 0 to 7.
3:0	ADDR_LSB	Set or return the 4LSB of PMBUS address. When bit [7] = 1'b0, the PMBus address 4LSB is set by ADDR pin voltage. Bit[3:0] returns the PMBus 4LSB address. When bit [7] = 1'b1, the 4LSB of PMBus is set with bit [3:0].

For example, when MFR_ADDR_PMBUS (EDh)=0xA0, it means PMBus address is 20h and 4LSB is set from register.

When MFR_ADDR_PMBUS (EDh)=0x20, it means PMBus address is 20h and set by ADDR pin voltage.

MFR_PG_RDL (EEh)

The MFR_ PG_RDL command on page0 is used to set the rail1 power good delay time.

Command	MFR_PG_RDL															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	X	X	PG_DELAY_TIME									

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates writes are ignored and always read as 0.
9:0	PG_DELAY_TIME	Set the rail1 PG indication delay time. 5us/LSB.

For example, to get 1ms PG low to high delay time, set MFR_PG_RDL (EEh)=0x00C8.

VENDOR_ID (EFh)

VENDOR_ID command returns the uniquely identifies for VR vendor. The vendor ID is assigned by Intel. MPS is assigned as 0x25.This register is mandatory and the value in it is fixed to 0x25.

Command	VENDER_ID							
Format	Unsigned Binary							
BIT	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r
Function	VENDER_ID							

Bits	Bit Name	Description
7:0	VENDOR_ID	Return the vendor ID of the mEZD81260A. The value is fixed to 0x25.

PRODUCT_ID (F0h)

PRODUCT_ID command returns the uniquely identifies for the VR product. The product ID is assigned by VR vendor. For the mEZD81260A, the product ID is assigned as 0x51. This register is mandatory and the value in it is fixed to 0x51.

Command	PRODUCT_ID							
Format	Unsigned Binary							
BIT	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r
Function	PRODUCT_ID							

Bits	Bit Name	Description
7:0	PRODUCT_ID	Return the product ID of the mEZD81260A. The value is fixed to 0x51.

CONFIG_ID (F1h)

CONFIG_ID provides the configuration code identifier for the register settings stored in EEPROM. MPS provides four digital codes “xxxx” for each application. The mEZD81260A full part number includes these four digits as a suffix, i.e., mEZD81260A -xxxx. Each “x” means a hexadecimal value between 0 & F. the higher two digits is fixed to “00”.The lower two digits are set in register CONFIG_ID.

Command	CONFIG_ID							
Format	Unsigned Binary							
BIT	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	CONFIG_ID							

Bits	Bit Name	Description
7:0	CONFIG_ID	Set the lower 2 digits of configuration code ID.

For example, the CONFIG_ID (F1h)=0x11, the configuration ID is 0011, and the full part number is mEZD81260A -0011.

When use MPS mEZD81260A GUI to configure the device, if the CONFIG_ID in configuration file doesn’t match with the value in the pre-programmed EEPROM, the configuration file won’t be able to load into the device.

MFR_PSI_SET (F2h)

The MFR_ PSI_SET command on page0 is used to set the power state for rail1.

Command	MFR_PSI_SET							
Format	Unsigned Binary							
BIT	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	POWER_STATE_SEL			

Bits	Bit Name	Description
7:4	RESERVED	Unused. X indicates writes are ignored and always read as 0.
3:1	POWER_STATE_SEL	Set the power state when auto power mode is disabled (register F2h, bit0=0) 3’b001: PS2, 1-phase DCM; 3’b01X: PS1, 1-phase CCM; 3’b1XX: PS0, 2-phase CCM; X means don’t care.
0	FORCE_PS_EN	Forcing power sate enable bit. 1’b0: disable forcing power state function, the mEZD81260A runs at auto power mode; 1’b1: enable forcing power state function. The power sate is determined by POWER_STATE_SEL (bit [3:1]).

MFR_PSI_ENTER (F3h)

The MFR_ PSI_ENTER command on page0 is used to set the power state dropping threshold at auto power mode. Auto power mode is enabled by set command MFR_PSI_SET (F2h), bit 0=0.

Command	MFR_PG_RDL															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X		MFR_PS1_LOW						MFR_PS0_LOW							

Bits	Bit Name	Description
15	RESERVED	Unused. X indicates writes are ignored and always read as 0.
14	DCM_DIS	A bit which is used to always disabled DCM at auto power mode. **The setting is effective for both rails.** 1'b0: enable DCM at auto power mode; 1'b1: disabled DCM at auto power mode.
13:8	MFR_PS1_LOW	Set the power state transition current threshold from 1-phase CCM to 1-phase DCM. It is only effective for rail1 at auto power mode. 0.5A/LSB.
7:0	MFR_PS0_LOW	Set the power state transition current threshold from 2-phase CCM to 1-phase CCM. It is only effective for rail1 at auto power mode. 0.5A/LSB.

MFR_PS_HYS (F4h)

The MFR_PS_HYS is used to set the rail1 power sate transition hysteresis value at auto power mode.

Command	MFR_PS_HYS							
Format	Unsigned Binary							
BIT	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	MFR_PS_HYS			

Bits	Bit Name	Description
7:4	RESERVED	Unused. X indicates writes are ignored and always read as 0.
3:0	MFR_PS_HYS	Set the power state transition threshold hysteresis. The power sate rising threshold can be calculated with: $(MFR\_PS_n\_ENTER + MFR\_PS\_HYS) \times 0.5A$ Where, n is the power state number, n=0 or 1. 0.5A/LSB

For example, when the mEZD81260A works at dual phase output mode, with MFR_PSI_ENTER (F3h) =0x0414, MFR_PS_HYS (F4h) =0x08, it means 2-phase CCM to 1-phase CCM entry threshold is 10A, and 1-phase CCM to 1-phase DCM threshold is 2A, with 4A power state rising hysteresis.

MFR_SAMP_LPF (F6h)

The MFR_ SAMP_LPF command is used to set the ADC sampling filter parameters for V_{OUT} sensing and IOUT reporting.

Command	MFR_SAMP_LPF							
Format	Unsigned Binary							
BIT	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	VOUT_ADC_LPF		IOUT_ADC_LPF		

Bits	Bit Name	Description
7:5	RESERVED	Unused. X indicates writes are ignored and always read as 0.
4:3	VOUT_ADC_LPF	Set the low pass filter parameter of V_{OUT} ADC sensing. The sensed output voltage is used for DC loop calibration internal the device. 2'b00: disable V_{OUT} ADC sensing low pass filter; 2'b01: 2 ADC sampling cycles; 2'b10: 4 ADC sampling cycles; 2'b11: 8 ADC sampling cycles;
2:0	IOUT_ADC_LPF	Set the low pass filter parameter of I_{OUT} ADC sensing. The sensed output current is used for I_{OUT} report. 3'b000: disabled I_{OUT} ADC sensing low pass filter; 3'b001: 2 ADC sampling cycles; 3'b010: 4 ADC sampling cycles; 3'b011: 8 ADC sampling cycles; 3'b100: 16 ADC sampling cycles; 3'b101: 32 ADC sampling cycles; 3'b110: 64 ADC sampling cycles; 3'b111: 128 ADC sampling cycles.

MFR_VR_CONFIG_ADV (F7h)

The MFR_ VR_CONFIG_ADV is used to configure some basic function of the mEZD81260A.

Command	MFR_VR_CONFIG_ADV															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X															

Bits	Bit Name	Description
15	RESERVED	Unused. X indicates writes are ignored and always read as 0.
14	TEST_MODE3	A test mode enable bit. At normal operation, always set it to **0**.
13	VREF_1/2DIVIDER_EN	Reference voltage 1/2 divider enable bit. On the mEZD81260A, VFB has a 1/2 divider buffer to divider to ADC sensing input. To match this 1/2 dividing ratio, the reference voltage for DC loop calibration is also divided by half. For normal operation, set bit 13=1. 1/b0: disable VREF 1/2 divider. When DC loop is enabled, the output voltage is 2x of the voltage setting with command VOUT_COMMAND (21h). 1'b1: enable VREF 1/2 divider.
12:11	BG_CHOP_MODE	Select the band gap chop frequency. Set to 500kHz at normal operations. The other options are for test mode. 2'b00: disable band gap chop; 2'b01: 125KHz; 2'b10: 250KHz; 2'b11: 500KHz.
10:9	DVID_RISE_STEP_R2	Set the extra VID step count for rail2 when DVID up. The extra VID steps are used to compensate the droop voltage drop caused the output capacitor charging during DVID up. 2'b00: 0 step; 2'b01: 1 step; 2'b10: 2 steps; 2'b11: 3 steps.
8:7	DVID_RISE_STEP_R1	Set the extra VID step count for rail1 when DVID up. The extra VID steps are used to compensate the droop voltage drop caused the output capacitor charging during DVID up. 2'b00: 0 step; 2'b01: 1 step; 2'b10: 2 steps; 2'b11: 3 steps.
6	VID-DAC_FILTER_EN_R2	Add VID-DAC output filter when DVID downward to avoid the output voltage undershoot. 1'b0: disable VID-DAC filter for rail2; 1'b1: enable VID-DAC filter for rail2.
5:4	VID-DAC_FILTER_SEL_R2	Program the rail2 VID-DAC output filter time. 2'b00:1us; 2'b01:3us; 2'b10:5us; 2'b11:7us.
3	VID-DAC_FILTER_EN_R1	Add VID-DAC output filter when DVID downward to avoid the output voltage undershoot. 1'b0: disable VID-DAC filter for rail1; 1'b1: enable VID-DAC filter for rail1.
2:1	VID-DAC_FILTER_SEL_R1	Program the rail1 VID-DAC output filter time. 2'b00:1us; 2'b01:3us; 2'b10:5us; 2'b11:7us.
0	DELAY_LINE_LOOP_EN	Delay line loop (DLL) enable bit. The mEZD81260A provides a DLL to reduce the PWM TON time resolution. 1'b0: disable DLL, T_{ON} with 5ns/LSB; 1'b1: enable DLL, T_{ON} with 0.625ns/LSB.

CLEAR_EEPROM_FAULTS (FFh)

The CLEAR_EEPROM_FAULTS command is used to clear the EEPROM CRC fault that occurs in copy EEPROM process. It is a written only command. There is no data byte for this command.

Page1 Register Map

PAGE (00h)

The PAGE command provides the ability to configure, control and monitor through only one physical address for both rails and the test mode.

Command	PAGE							
Format	Unsigned binary							
BIT	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	X	X	PAGE	

Bits	Bit Name	Description
7:2	RESERVED	Unused. X indicates writes are ignored and always read as 0.
1:0	PAGE	2'b00: Page0, all commands address rail1 2'b01: Page1, all commands address rail2 Others: In-effective input

OPERATION (01h)

The OPERATION command on page1 is used to turn the rail2 output on/off in conjunction with input from the EN2 pin. It is also used to set the output voltage to the upper or lower MARGIN voltages. The rail2 stays in the command operating mode until a subsequent OPERATION command or a state altering of the EN2 pin change rail2 to another mode.

Command	OPERATION							
Format	Unsigned binary							
BIT	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r	r
Function	OPERATION_MODE							

Bits	Bit Name	Description
7:0	OPERATION_MODE	Set the operation mode for rail2. 7'b00xxxxxx: High-Z off 7'b01xxxxxx: Soft off 7'b1000xxxx:Normal on 7'b1001xxxx: Margin low 7'b1010xxxx: Margin high "x" means don't care.

CLEAR_FAULTS (03h)

The CLEAR_FAULTS command is used to clear the system fault after system initialization ends. CLEAR_FAULTS is written only and there is no data byte for it. It is effective for both rails no matter the value of PAGE command. The faults include VIN UVLO, VIN OVP, OTP, output OVP, UVP, OCP-Total protections, PMBus communication faults and EEPROM faults. Once send a CLEAR_FAULTS, the faults listed above on both rails are cleared and the fault bits in register MFR_FAULTS (86h) and MFR_CML (87h) are all reset if the associate fault is removed.

STORE_USER_ALL (15h)

The STORE_USER_ALL command instructs the PMBus device to copy the page0 and page1 values in the operating memory to the matching locations in the EEPROM. Any items in operating memory that do not have matching locations in the EEPROM are ignored.

It is permitted to use this command while the device is outputting power.

This command is written only. There is no data byte for this command.

RESTORE_USER_ALL (16h)

The RESTORE_USER_ALL command instructs the PMBus device to copy the page0 and page1 value of the EEPROM to the matching locations in the operating memory. The values in the operating memory are overwritten by the value retrieved from the EEPROM. Any items in the EEPROM that do not have matching locations in the operating memory are ignored.

It is **NOT** permitted to use this command while the device is outputting power, or the command will be ignored.

This command is written only. There is no data byte for this command.

VOUT_COMMAND (21h)

The VOUT_COMMAND on page1 sets the rail2 nominal output voltage value in VID format.

Command	VOUT_COMMAND															
Format	VID															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	X	X	VOUT_VID									

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates writes are ignored and always read as 0.
9:0	VOUT_VID	Set the Rail2 nominal output voltage level in VID format. 5mV/LSB.

VOUT_TRIM (22h)

The VOUT_TRIM command on page1 is used to apply an offset value to the rail2 reference voltage (VREF). It is generally used by the end users to trim the output voltage at the time the PMBus device is assembled into the end user's system. It also can be used to fine tune the output voltage when the designed VREF is output 5mV step.

Command	VOUT_TRIM															
Format	Signed binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	X	X	X	X	X	X	X	X	VREF_TRIM			

Bits	Bit Name	Description
15:4	RESERVED	Unused. X indicates writes are ignored and always read as 0.
2:0	VREF_TRIM	Add a fixed offset over the VREF of rail2. 3.13mV/LSB. It is in twos compliment format. Bit[3] is the sign bit. The voltage list below shows the direct value and real world value. 4'b0000: 0mV 4'b0001: +3.13mV 4'b0111: +21.91mV 4'b1000: 0mV 4'b1001: -21.91mV 4'b1111: -3.13mV

VOUT_MARGIN_HIGH (25h)

The VOUT_MARGIN_HIGH command sets the margin high voltage level to which the output is to be changed when the OPERATION command is set to “Margin High”.

Command	VOUT_MARGIN_HIGH															
Format	VID															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	X	X	VOUT_MARGIN_HIGH									

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates writes are ignored and always read as 0.
9:0	VOUT_MARGIN_HIGH	Set the Rail2 margin high state output voltage level. 5mV/LSB.

VOUT_MARGIN_LOW (26h)

The VOUT_MARGIN_LOW command sets the margin low voltage level to which the output is to be changed when the OPERATION command is set to “Margin Low”.

Command	VOUT_MARGIN_LOW															
Format	VID															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	X	X	VOUT_MARGIN_LOW									

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates writes are ignored and always read as 0.
9:0	VOUT_MARGIN_LOW	Set the Rail2 margin low state output voltage level. 5mV/LSB.

VOUT_SCALE_LOOP (29h)

The VOUT_SCALE_LOOP command on page1 sets the rail2 output voltage to reference voltage dividing ratio.

Command	VOUT_SCALE_LOOP															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	X	X	X	X	VOUT_SCALE_LOOP							

Bits	Bit Name	Description
15:8	RESERVED	Unused. X indicates writes are ignored and always read as 0.
7:0	VOUT_SCALE_LOOP	Set the rail2 output voltage to reference voltage VREF dividing ratio with the following equation. VREF ranges from 0.245-1.52V. $VOUT\_SCALE\_LOOP = 128 \times \frac{V_{REF}}{V_{OUT}}$

For example, to support 5V output voltage, select VREF=0.82V, then VOUT_SCALE_LOOP (29h) = 0x0015.

FREQUENCY_SWITCH (33h)

The FREQUENCY_SWITCH command on page1 is used to set the switching frequency for rail2. The switching frequency range is from 200KHz to 2MHz, with 10KHz per step.

Command	FREQUNCY_SWITCH															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	X	X	X	X	SWITCH_FREQUENCY							

Bits	Bit Name	Description
15:8	RESERVED	Unused. X indicates writes are ignored and always read as 0.
7:0	SWITCH_FREQUENCY	Set the rail2 switching frequency from 200-2000KHz. 10KHz/LSB.

TON_DELAY (60h)

The TON_DELAY command on page1 is used to set the rail2 power on delay time.

Command	TON_DELAY															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	TON_DELAY															

Bits	Bit Name	Description
15:0	TON_DELAY	Set the rail2 power on delay time. The power on delay time starts when the system initialization is completed. When the Ton delay time is over, rail2 begins soft-starts. 100us/LSB.

For example, to get 10ms power on delay time, set TON_DELAY (60h)=0x0064.

TON_RISE (61h)

The TON_RISE command on page1 is used to set the rail2 VREF soft-start slew rate. Figure-15 shows the definition of sub-registers in TON_RISE.

The output voltage soft-start slew rate can be calculated with Equation (17):

$$VOUT\_SR = \frac{(VID\_STEP+1)\times 5mV}{(VID\_SR\_CNT+1)\times 200ns}\times\frac{1}{K_{R2}} \quad (17)$$

Where,

K_{R2} is the rail2 output divider ratio.

Command	TON_RISE															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	VID_STEP		VID_SR_CNT										

Bits	Bit Name	Description
15:13	RESERVED	Unused. X indicates writes are ignored and always read as 0.
12:11	VID_STEP	At soft-start, VREF is rising step by step. VID_STEP sets the VREF amplitude for each step in VID format. The VREF per step can be calculated with: (VID_STEP+1)*5mV. 5mV/LSB.
10:0	VID_SR_CNT	Set the duration time for each VREF step. The time can be calculated with equation: (SS_SR_CNT+1)*200ns. 200ns/LSB.

For example, if VID_STEP= 2'b00, DVID_SR_CNT=0, the soft start slew rate is 25mV/us.

TOFF_DELAY (64h)

The TOFF_DELAY command on page1 is used to set the rail2 power off delay time. Power off delay time is only effective at OPERATION command soft-off.

Command	TOFF_DELAY															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	TOFF_DELAY															

Bits	Bit Name	Description
15:0	TOFF_DELAY	Set the rail2 power off delay time at OPERATION command soft-off. 100us/LSB.

TOFF_FALL (65h)

This TOFF_FALL command is used to set the DVID and soft-shutdown slew rate.

Command	TOFF_FALL															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	VID_STEP		VID_SR_CNT										

Bits	Bit Name	Description
15:13	RESERVED	Unused. X indicates writes are ignored and always read as 0.
12:11	VID_STEP	At dynamic VID transition and soft off, VREF is changing step by step. VID_STEP sets the VREF amplitude for each step in VID format. The VREF per step can be calculated with: (VID_STEP+1)*5mV. 5mV/LSB.
10:0	VID_SR_CNT	Set the duration time for each VREF step. The time can be calculated with equation: (VID_SR_CNT+1)*200ns. 200ns/LSB.

READ_VOUT (8Bh)

The READ_VOUT command on page1 is used to return the ADC sensed VDIFF voltage on rail2. Then the PMBus reported output voltage can be calculated with Equation (18):

$$VOUT\_REPORT = \frac{3.13\ (mV) \times READ\_VOUT}{K_{R2}} \quad (18)$$

Command	READ_VOUT															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	X	X	READ_VOUT									

Bits	Bit Name	Description
15:7	RESERVED	Unused. X indicates writes are ignored and always read as 0.
6:0	READ_VOUT	Return the ADC sensed voltage on rail2 VDIFF1 pin. 3.13mV/LSB.

MFR_CS (8Fh)

The MFR_CS command on page1 is used to monitor the phase1 average inductor current.

Command	MFR_CS							
Format	Unsigned binary							
BIT	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	READ_IPHASE						

Bits	Bit Name	Description
7	RESERVED	Unused. X indicates writes are ignored and always read as 0.
6:0	READ_IPHASE	Return the sensed phase1 average current. 0.5A/LSB.

MFR_OCP_TOTAL_SET (D6h)

The MFR_OCP_TOTAL_SET command on page1 is used to set the rail2 total current protection level, protection mode and OCP blanking time. OCP_Total is a time based over current protection. It should be tripped when the sensed average output current exceeds the threshold for a period of time. This period of time is referred as OCP blanking time. The OCP_Total can be programmed to No Action, Hiccup, Retry 6-Time and Latch-Off mode via PMBus.

Command	MFR_OCP_TOTAL_SET															
Format	Binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	MODE		OCP_BLANKING_TIME					OCP_LIMIT_LSB					

Bits	Bit Name	Description
15:13	RESERVED	Unused. X indicates writes are ignored and always read as 0.
12:11	MODE	Set OCP-Total protection action mode. There are four modes available. 2'b00: No Action; 2'b01: Latch-Off; 2'b10: Hiccup; 2'b11: Retry 6-Time.

Bits	Bit Name	Description
10:6	OCP_BLANKING_TIME	Set OCP-Total protection blanking time. An OCP-Total fault is occurred if the current exceeds the OCP-TOTAL threshold for an OCP blanking time 100us/LSB.
5:0	OCP_LIMIT	Set the OCP-Total threshold. The OCP-Total threshold of rail2 ranges from 0 to 127A. 1A/LSB.

For example, when set MFR_OCP_TOTAL_SET=0x0965, the OCP_total current limit level is 30A, OCP_total protection mode is latch off with 500us OCP blanking time.

MFR_OVP_SET (D7h)

The MFR_OVP_SET command on page1 is used to set the rail2 output over voltage protection level, mode and blanking time.

Command	MFR_OVP_SET															
Format	Binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X		MODE		OVP_BLANKING_TIME`									

Bits	Bit Name	Description
15:13	RESERVED	Unused. X indicates writes are ignored and always read as 0.
12	VFB+_WINDOW_EN	VFB+ Window enable bit. VFB+ window is a VFB+25mV threshold. It is used for output overshot reduction and DC loop hold function. 1'b0: VFB+ Window is disabled; 1'b1: VFB+ Window is enabled.
11:10	OVP1_MODE	Set V_{OUT} OVP1 protection mode. There are four modes available. 2'b00: No Action; 2'b01: Latch-Off; 2'b10: Hiccup; 2'b11: Retry 6-Time.
9:4	OVP1_BLANKING_TIME	Set V_{OUT} OVP1 blanking time. An OVP fault is occurred if the sensed VDIFF exceeds the OVP1 threshold for an OVP blanking time 100ns/LSB.
3:2	OVP2_LIMIT	Set OVP2 threshold. OVP2 is a regulation type threshold. If the voltage on VDIFF exceeds the OVP2 threshold, the MEZD81260A turns on low side MOSFET to discharge output voltage below OVP2 threshold. 2'b00: VREF+100mV; 2'b01: VREF+200mV; 2'b10: VREF+300mV; 2'b11: VREF+400mV
1:0	OVP1_LIMIT	Set OVP1 threshold. OVP1 is a protection type threshold. If the voltage on VDIFF exceeds the OVP1 threshold, the mEZD81260A turns on low side MOSFET to discharge output voltage and takes action to Latch-Off, Hiccup or Retry 6-Time as programmed by OVP1_MODE. At No Action mode, the mEZD81260A keeps switching and the OVP fault bit in register MFR_FALUTS (86h) will not assert. Always design OVP1_LIMIT higher than OVP2_LIMIT. 2'b00: VREF+100mV; 2'b01: VREF+200mV; 2'b10: VREF+300mV; 2'b11: VREF+400mV.

For example, when set MFR_OVP_SET=0x1456, the OVP setting of rail2 is: Disable VFB+ window; OVP2 threshold is VREF+200mV; OVP1 threshold is VREF+300mV and the rail2 latches down once VDIFF1 exceeds OVP1 threshold for 500ns.

MFR_UVP_SET (D8h)

The MFR_UVP_SET command on page1 is used to set the rail2 under voltage protection mode, level and delay time.

Command	MFR_UVP_SET															
Format	Binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X													

Bits	Bit Name	Description
15:11	RESERVED	Unused. X indicates writes are ignored and always read as 0.
10	VFB-_WINDOW_EN	VFB- Window enable bit. VFB- window is a VFB-25mV threshold. It is can be used to expedite load transient response at APM mode. 1'b0: VFB- Window is disabled; 1'b1: VFB- Window is enabled.
9:8	UVP_MODE	Set V_{OUT} UVP protection action mode. There are four modes available. 2'b00: No Action; 2'b01: Latch-Off; 2'b10: Hiccup; 2'b11: Retry 6-Time.
7:2	UVP_BLANKING_TIME	Set V_{OUT} UVP blanking time. An UVP fault is occurred if the sensed VDIFF falls below the UVP threshold for an UVP blanking time 100ns/LSB.
1:0	UVP_LIMIT	Set UVP threshold. If the voltage on VDIFF falls below the UVP threshold, the mEZD81260A takes no action or acts to Latch-Off, Hiccup or Retry 6-Time as programmed by UVP_MODE. At No Action mode, the MEZD81260A keeps switching and the UVP fault bit in register MFR_FALUTS (86h) will not assert. 2'b00: VREF+100mV; 2'b01: VREF+200mV; 2'b10: VREF+300mV; 2'b11: VREF+400mV.

MFR_OCP_PHASE_SET (DAh)

The MFR_OCP_PHASE_SET command on page1 is used to set the **phase2** OCP-Phase current limit. OCP-Phase is a single phase valley current limitation threshold. The mEZD81260A monitors phase current cycle-by-cycle. When the phase current exceeds the OCP-Phase threshold at PWM off time, PWM keeps low to discharge inductor current below the set threshold. he OCP valley current is calculate with equation (14).

Command	MFR_OCP_PHASE_SET															
Format	Binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	X	X	X	X	OCP_PHASE_LIMIT							

Bits	Bit Name	Description
15:8	RESERVED	Unused. X indicates writes are ignored and always read as 0.
7:0	OCP_PHASE_LIMIT	Set the per phase valley current limit threshold.

MFR_MIN_OFF_TIME (E1h)

The MFR_MIN_OFF_TIME command is used to set the minimum off time of each phase. The minimum off time limits switching frequency. It is active for both rails.

Command	MFR_MIN_OFF_TIME							
Format	Direct							
BIT	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	MIN_OFF_TIME				

Bits	Bit Name	Description
7:5	RESERVED	Unused. X indicates writes are ignored and always read as 0.
4:0	MIN_OFF_TIME	Set the minimum off time of each phase. 5ns/LSB.

MFR_SLOPE_SR_PS1 (E4h)

The MFR_SLOPE_SR_PS1 command on page1 is used to set the slew rate of slope compensation for rail2 at PS1 (1-phase CCM).

Command	MFR_SLOPE_SR_PS1							
Format	Direct							
BIT	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	CURRENT_SOURCE					

Bits	Bit Name	Description
7:6	RESERVED	Unused. X indicates writes are ignored and always read as 0.
7:0	CURRENT_SOURCE	Set the current source value for slope compensation at PS1. The current source can be calculated with: $CURRENT\_SOURCE \times 0.25\mu A$

The capacitance for slope compensation is 29.6pF

MFR_SLOPE_CNT_PS1 (E5h)

The MFR_SLOPE_CNT_PS1 command on page1 is used to set the slope voltage clamp time at PS1 (1-phase CCM). The slope clamp time for PS1 can be calculated with equation (20).

Command	MFR_SLOPE_CNT_PS1															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	X	X	SLOPE_CNT									

Bits	Bit Name	Description
15:9	RESERVED	Unused. X indicates writes are ignored and always read as 0.
8:6	SLOPE_CNT	Set the slope clamp timer for PS1. 5ns/LSB.

MFR_SLOPE_SR_PS2 (E6h)

The MFR_SLOPE_SR_PS2 command on page1 is used to set the slew rate of slope compensation for rail2 at PS2 (1-phase DCM). The slope capacitance is fixed with 29.6pF.

Command	MFR_SLOPE_SR_PS2							
Format	Direct							
BIT	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	CURRENT_SOURCE					

Bits	Bit Name	Description
7:6	RESERVED	Unused. X indicates writes are ignored and always read as 0.
5:0	CURRENT_SOURCE	Set the current source value for slope voltage generation at PS2. The current source can be calculated with: $CURRENT\_SOURCE \times 0.25\mu A$

MFR_SLOPE_CNT_PS2 (E7h)

The MFR_SLOPE_CNT_PS2 command on page1 is used to set the slope voltage clamp time at PS2 (1-phase DCM). The slope clamp time can be calculated with equation 21.

Command	MFR_SLOPE_CNT_PS2							
Format	Direct							
BIT	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	SLOPE_CNT					

Bits	Bit Name	Description
7:6	RESERVED	Unused. X indicates writes are ignored and always read as 0.
5:0	SLOPE_CNT	Set the slope clamp time for PS2. 80ns/LSB.

MFR_SLOPE_SR_F25K (EAh)

The MFR_SLOPE_SR_F25K command on page1 is used to set the slope compensation slew rate for rail2 at ultra-sonic mode. This slope compensation takes action before each PWM on pulse when the switching cycle is limited to 40us.The slope capacitance is fixed with 3.9pF.

Command	MFR_SLOPE_SR_PS1							
Format	Direct							
BIT	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	CURRENT_SOURCE					

Bits	Bit Name	Description
7:6	RESERVED	Unused. X indicates writes are ignored and always read as 0.
5:0	CURRENT_SOURCE	Set the current source value for slope voltage generation at ultra-sonic mode. The current source can be calculated with: $CURRENT\_SOURCE \times 0.25\mu A$

In general designs, set CURRENT_SOURCE=2 to make the PWM on pulse stable at ultra-sonic mode.

MFR_PS1_TRIM (EBh)

The MFR_ PS01_TRIM command on page1 is used to trim the output voltage at 2-phase CCM (PS0) and 1-phase CCM (PS1) of rail2.

Command	MFR_PS01_TRIM															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	X	X	X	X	X		VTRIM_PS1					

Bits	Bit Name	Description
15:7	RESERVED	Unused. X indicates writes are ignored and always read as 0.
6	AUTO_VTRIM_EN	Power state automatic trim function enable bit at force power state mode. 1'b0: disable to trim reference voltage automatically for each power state. 1'b1: enable to trim reference voltage automatically for each power state.
5:0	VTRIM_PS1	Set the reference voltage trim for PS0. 1.37mV/LSB

MFR_PS2_TRIM (ECh)

The MFR_ PS2_TRIM command on page1 is used to trim the output voltage at 1-phase DCM (PS2)

Command	MFR_PS2_TRIM															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	X	X	X	X	X	X	X	VTRIM_PS2				

Bits	Bit Name	Description
15:5	RESERVED	Unused. X indicates writes are ignored and always read as 0.
4:0	VTRIM_PS2	Set the reference voltage trim for PS0. 1.37mV/LSB

MFR_PG_RDL (EEh)

The MFR_ PG_RDL command on page1 is used to set the rail2 power good delay time.

Command	MFR_PG_RDL															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	X	X	PG_DELAY_TIME									

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates writes are ignored and always read as 0.
9:0	PG_DELAY_TIME	Set the rail2 PG indication delay time. 5us/LSB.

MFR_PSI_SET (F2h)

The MFR_ PSI_SET command on page1 is used to set the power state for rail2.

Command	MFR_PSI_SET							
Format	Unsigned Binary							
BIT	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	X	POWER_STATE_SEL		

Bits	Bit Name	Description
7:3	RESERVED	Unused. X indicates writes are ignored and always read as 0.
2:1	POWER_STATE_SEL	Set the power state when auto power mode is disabled (register F2h, bit0=0) 2'b01: PS2, 1-phase DCM; 2'b1X: PS1, 1-phase CCM; X means don't care.
0	FORCE_PS_EN	Forcing power sate enable bit. 1'b0: disable forcing power state function, the mEZD81260A runs at auto power mode; 1'b1: enable forcing power state function. The power sate is determined by POWER_STATE_SEL (bit [2:1]).

MFR_PSI_ENTER (F3h)

The MFR_ PSI_ENTER command on page1 is used to set the power state dropping threshold at auto power mode. Auto power mode is enabled by set command MFR_PSI_SET (F2h), bit 0=0.

Command	MFR_PG_RDL															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	X	X	X	X	X	MFR_PS1_LOW						

Bits	Bit Name	Description
15:7	RESERVED	Unused. X indicates writes are ignored and always read as 0.
6:0	MFR_PS1_LOW	Set the power state transition current threshold from 2-phase CCM to 1-phase CCM. It is only effective for rail2 at auto power mode. 0.5A/LSB.

MFR_PS_HYS (F4h)

The MFR_PS_HYS is used to set the rail2 power sate transition hysteresis value at auto power mode.

Command	MFR_PS_HYS							
Format	Unsigned Binary							
BIT	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	MFR_PS_HYS			

Bits	Bit Name	Description
7:4	RESERVED	Unused. X indicates writes are ignored and always read as 0.
3:0	MFR_PS_HYS	Set the power state transition threshold hysteresis. The power sate rising threshold can be calculated with: $(MFR\_PS_n\_ENTER + MFR\_PS\_HYS) \times 0.5A$ Where, n is the power state number, n=0 or 1. 0.5A/LSB

For example, when the module works at dual phase output mode, with MFR_PSI_ENTER (F3h) =0x0414, MFR_PS_HYS (F4h) =0x08, it means 2-phase CCM to 1-phase CCM entry threshold is 10A, and 1-phase CCM to 1-phase DCM threshold is 2A, with 4A power state rising hysteresis.

MFR_FAULTS_RECORD (F8h)

The MFR_FAULTS command is used to return the VR operation faults at last power cycle. When MFR_PRT_SET (DCh), bit4=1, the faults type will be stored into EEPROM when a fault occurs. The fault type will be restored into F8h on next power on cycle.

Command	MFR_FAULTS_RECORD															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	X	X	X									

Bits	Bit Name	Description
15:9	RESERVED	Unused. X indicates writes are ignored and always read as 0.
8	IOUT_OC _R2	Rail2 OCP-Total fault indication bit. 1'b0: no OCP-Total fault on rail2; 1'b1: OCP-Total fault has occurred on rail2.
7	IOUT_OC _R1	Rail1 OCP-Total fault indication bit. 1'b0: no OCP-Total fault on rail1; 1'b1: OCP-Total fault has occurred on rail1.
6	VOUT_UV _R2	Rail2 V_{OUT} UV fault indication bit. It is set when rail2 V_{OUT} UVP blanking time ends and V_{OUT} UV still exists. 1'b0: no V_{OUT} UV fault on rail2; 1'b1: V_{OUT} UV fault has occurred on rail2.
5	VOUT_UV _R1	Rail1 V_{OUT} UV fault indication bit. It is set when rail1 V_{OUT} UVP blanking time ends and V_{OUT} UV still exists. 1'b0: no V_{OUT} UV fault on rail1; 1'b1: V_{OUT} UV fault has occurred on rail1.

Bits	Bit Name	Description
4	VOUT_OV _R2	Rail2 V_{OUT} OV fault indication bit. It is set when rail2 V_{OUT} OVP blanking time ends and V_{OUT} OV still exists. 1'b0: no V_{OUT} OV fault on rail2; 1'b1: V_{OUT} OV fault has occurred on rail2.
3	VOUT_OV _R1	Rail1 V_{OUT} OV fault indication bit. It is set when rail1 V_{OUT} OVP blanking time ends and V_{OUT} OV still exists. 1'b0: no V_{OUT} OV fault on rail1; 1'b1: V_{OUT} OV fault has occurred on rail1.
2	OT_FLT	Over temperature fault indication bit. 1'b0: no OT fault has occurred; 1'b1: OT fault has occurred.
1	VIN_OV	V_{IN} OV fault indication bit. 1'b0: no V_{IN} OV fault has occurred; 1'b1: V_{IN} OV fault has occurred.
0	VIN_UV	V_{IN} UV fault indication bit. 1'b0: no V_{IN} UV fault has occurred; 1'b1: V_{IN} UV fault has occurred.

CLEAR_EEPROM_FAULTS (FFh)

The CLEAR_EEPROM_FAULTS command is used to clear the EEPROM CRC fault that occurs in copy EEPROM process. It is a written only command. There is no data byte for this command.

TYPICAL APPLICATION CIRCUITS

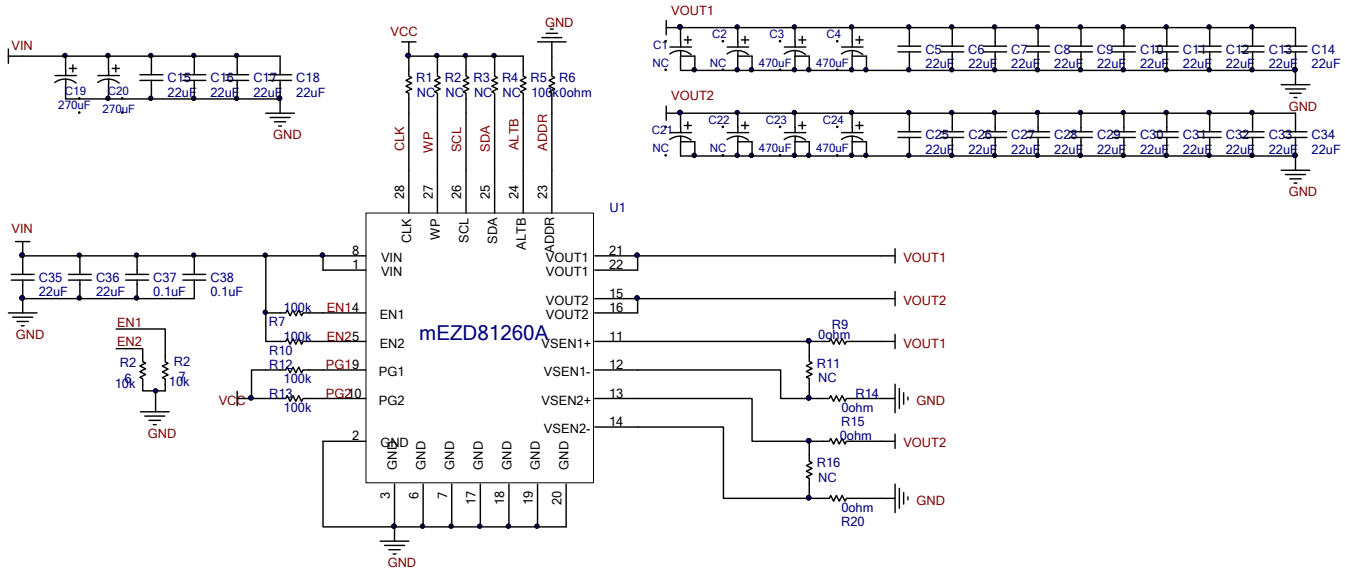


Figure 2: 12V$_{IN}$, 2 rails mode

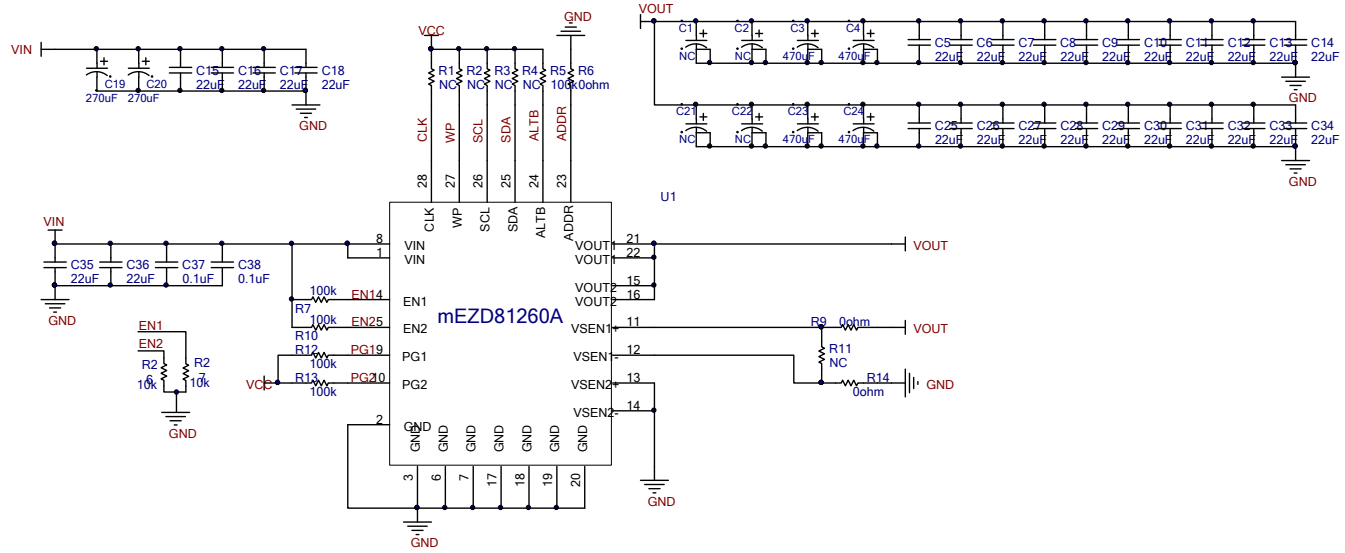
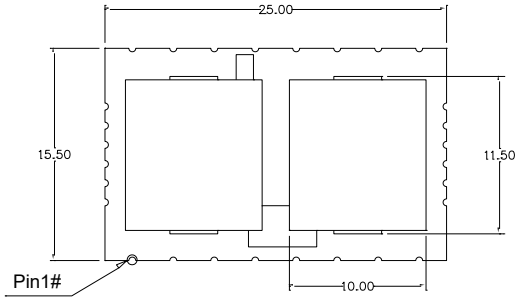


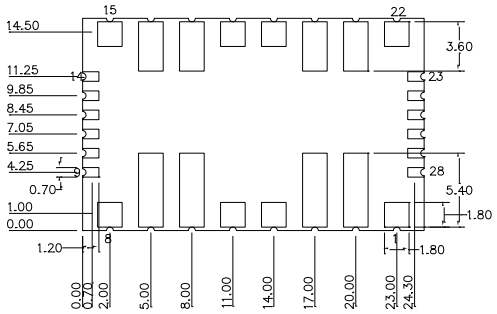
Figure 3: 12V$_{IN}$, 2 phases mode

PACKAGE INFORMATION

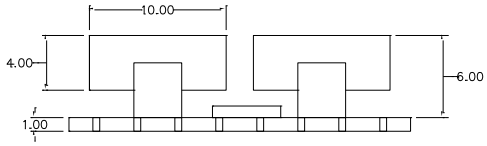
LGA (25mmx15.5mmx7 mm)



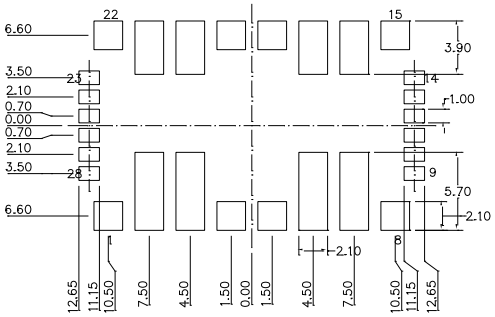
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

