MPQ8875A – 36V, 5A, 4-Switch Synchronous Buck-Boost Converter

Application Note

Prepared by
Automotive Product Line

January 2021

TABLE OF CONTENTS

ABSTRACT

This application note presents the circuit design and associated external components guide for the MPQ8875A, a 36V, 5A, automotive, four-switch, synchronous buck-boost converter. The wide 2.2V to 36V input voltage range makes it well-suited for a variety of multi-purpose automotive and industrial applications. Proprietary constant-on-time (COT) control and a fully integrated four-switch configuration allow the converter to flexibly change its topology between buck, boost, and buck-boost to optimize performance and efficiency with input voltages that are above, below, or even equal to the output voltage.

1 INTRODUCTION

The MPQ8875A is a 36V, 5A, automotive, four-switch, synchronous buck-boost converter. The wide input voltage range makes it well-suited for a variety of multi-purpose automotive and industrial applications. Four integrated, low-resistance N-channel MOSFETs minimize the size of the external circuitry and allow the converter to regulate the output voltage (V_{OUT}) with input voltages (V_{IN}) above, below, or equal to V_{OUT}. The flexible topology transitions reduce power losses to maximize efficiency. In addition, the proprietary constant-on-time (COT) control algorithm ensures seamless transitions between the adjacent operational regions. The MPQ8875A can operate at switching frequencies from 200kHz to 2.2MHz, allowing applications to be optimized for board size, efficiency, and EMI performance. Furthermore, the most electrical characteristics are programmable by accessing the related internal registers via the I^2C interface.

2 COMPONENT SIZING

2.1 MPQ8875A Operation

The MPQ8875A is a four-switch buck-boost converter. The mode is based on the measured V_{IN} and V_{OUT}. In order to successfully transition modes, the duty cycle must not fall below the minimum or exceed the maximum. Transition points must be achievable by both modes.

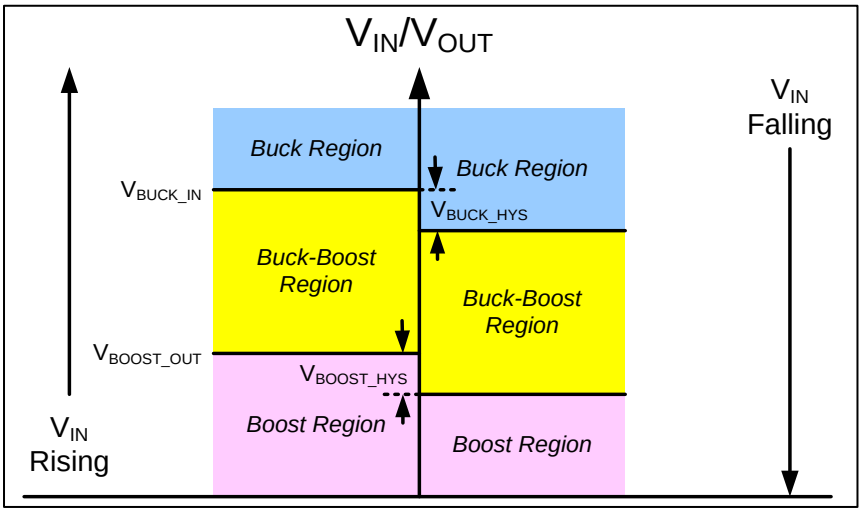

Figure 1: MPQ8875A V_{IN}/V_{OUT}

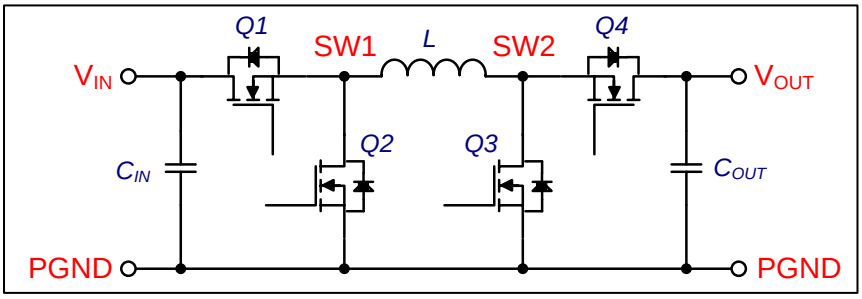

Figure 2: MPQ8875A Four-Switch Buck/Boost

In buck mode, Q4 is 100%, while Q1 and Q2 vary to regulate the output. In boost mode, Q1 is 100%, while Q3 and Q4 vary to regulate the output. In buck-boost mode, Q3 and Q4 have a fixed duty cycle while Q1 and Q2 vary to regulate the output.

2.2 Duty Cycle

The duty cycle depends on the input voltage, output voltage, and operating mode. The duty cycle for the buck region can be calculated with Equation (1):

$$D = \frac{V_{OUT}}{V_{IN}} \quad (1)$$

The duty cycle for the buck-boost region can be calculated with Equation (2):

$$D_{BUCK} = \frac{V_{OUT}}{V_{IN}}(1 - D_{BOOST}) \quad (2)$$

Where D_{BOOST} is a programmable constant.

The duty cycle for the boost region can be calculated with Equation (3):

$$D = 1 - \frac{V_{IN}}{V_{OUT}} \quad (3)$$

2.3 Switching Frequency

The MPQ8875A supports a 200kHz to 1000kHz frequency with 50kHz steps. Any frequency can be selected as the center frequency (i.e. 475kHz) for mass production (factory programmed). Higher frequencies can allow the user to reduce the size and number of external components, but also increases power loss. When syncing, set the free-running frequency to be below the minimum sync frequency.

Register 03h							
Bit 7 (R/W)	**Bit 6 (R/W)**	**Bit 5 (R/W)**	**Bit 4 (R/W)**	**Bit 3 (R/W)**	**Bit 2 (R/W)**	**Bit 1 (R/W)**	**Bit 0 (R/W)**
SYNC1	SYNC0	FSW5	FSW4	FSW3	FSW2	FSW1	FSW0

Bit Field Definitions

Bits	Field Name	Description
7:6	SYNC[1:0]	Sets the synchronization mode. 00h: Disabled 01h: Synchronized clock input 02h: Synchronized clock output (with 0° phase shift) 03h: Synchronized clock output (with 180° phase shift)
5:0	FSW[5:0]	Sets the switching frequency (f_{SW}) of the converter. Although FSW[5:0] can be set up to 2.2MHz, the maximum f_{SW} supported by the MPQ8875A is 1MHz. 00h to 03h: f_{SW} = Reserved 03h to 2Bh: f_{SW} = FSW[5:0] x 50kHz (resolution = 50kHz) 2Ch to 3Fh: f_{SW} = 2.2MHz

2.4 Transition Thresholds and Boost On Time

Register 09h							
Bit 7 (R/W)	**Bit 6 (R/W)**	**Bit 5 (R/W)**	**Bit 4 (R/W)**	**Bit 3 (R/W)**	**Bit 2 (R/W)**	**Bit 1 (R/W)**	**Bit 0 (R/W)**
BKHYS1	BKHYS0	BKIN1	BKIN0	BSTHYS1	BSTHYS0	BSTOUT1	BSTOUT0

Bit Field Definitions

Bits	Field Name	Description
7:6	BKHYS[1:0]	Sets the transition hysteresis between buck and buck-boost modes. 00h: V_{IN} = 5% of V_{OUT} 01h: V_{IN} = 7.5% of V_{OUT} 02h: V_{IN} = 10% of V_{OUT} (invalid when BKIN[1:0] is set to 00h) 03h: V_{IN} = 12.5% of V_{OUT} (invalid when BKIN[1:0] is set to 00h)

5:4	BKIN[1:0]	Sets the threshold of buck-boost transferring to buck when V_{IN} rises. 00h: V_{IN} = 110% of V_{OUT} 01h: V_{IN} = 120% of V_{OUT} 02h: V_{IN} = 125% of V_{OUT} 03h: V_{IN} = 130% of V_{OUT}
3:2	BSTHYS[1:0]	Sets the transition hysteresis between boost and buck-boost modes. 00h: V_{IN} = 5% of V_{OUT} 01h: V_{IN} = 7.5% of V_{OUT} 02h: V_{IN} = 10% of V_{OUT} 03h: V_{IN} = 12.5% of V_{OUT}
1:0	BSTOUT[1:0]	Sets the threshold of boost transferring to buck-boost when V_{IN} rises. 00h: V_{IN} = 70% of V_{OUT} 01h: V_{IN} = 80% of V_{OUT} 02h: V_{IN} = 85% of V_{OUT} 03h: V_{IN} = 90% of V_{OUT}

Register 08h							
Bit 7 (R/W)	**Bit 6 (R/W)**	**Bit 5**	**Bit 4**	**Bit 3 (R/W)**	**Bit 2 (R/W)**	**Bit 1 (R/W)**	**Bit 0 (R/W)**
ADDR3	ADDR2	ADDR1	ADDR0	CYCEXTEN	RESERVED	BSTONT1	BSTONT0

Bit Field Definitions

Bits	Field Name	Description
7:4	ADDR[3:0]	Sets the I^2C bus address. The valid address is effective immediately once write command is accepted.
3	CYCEXTEN	Enables cycle extension in buck-boost mode. 0: Disabled 1: Enabled
2	RESERVED	Reserved.
1:0	BSTONT[1:0]	Sets the constant-on-time (COT) control of the boost switch in buck-boost mode (in % of t_{SW}). 00h: 20%; 01h: 30%; 02h: 40%; 03h: 50%

The four mode transitions are determined by the following thresholds:

- Buck to buck-boost: BKIN - BKHYS
- Buck-boost to buck: BKIN
- Boost to buck-boost: BSTOUT - BSTHYS
- Buck-boost to boost: BSTOUT

The threshold values are determined by REG09. The accuracy for most of these thresholds is about ±2%. The boost on time controls the conversion ratio in buck-boost mode (±20%).

Figure 3 shows which transition values will work for most applications that follow the guidance in this application note. Further optimization is possible; for details, contact an MPS FAE.

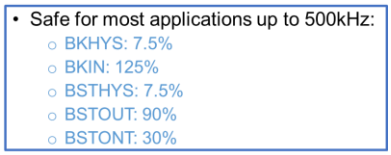

Figure 3: Recommended Mode Transition Thresholds

2.5 Selecting the Inductor

A 1µH to 10µH inductor with a DC current rating at least 25% greater than the maximum inductor current is recommended for most applications. Unlike buck and boost modes, the inductor current in buck-boost mode is not triangular (see Figure 4).

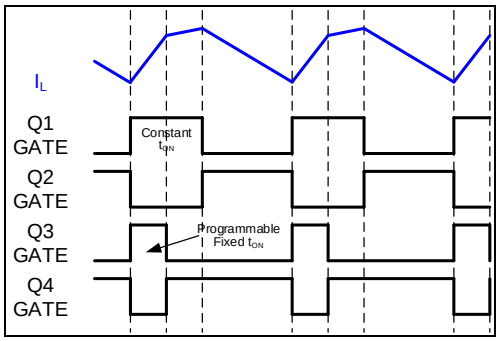

Figure 4: MPQ8875A CCM, Buck-Boost Mode in Normal Operation (V_{IN} > V_{OUT})

The worst-case inductor ripple occurs in buck-boost mode near the transition thresholds, calculated with Equation (4) and Equation (5):

$$V_{IN} \geq V_{OUT}: \Delta I_L = \frac{V_{OUT}}{f_{SW} \times L}(1 - D_{BUCK}) \quad (4)$$

$$V_{IN} < V_{OUT}: \Delta I_L = \frac{V_{IN}}{f_{SW} \times L}(D_{BOOST}) \quad (5)$$

It is recommended to keep the inductor ripple at or below 3A. The peak inductor current occurs in boost mode at the minimum V_{IN}, calculated with Equation (6):

$$I_{L\_PEAK} = \frac{V_{IN}(V_{OUT} - V_{IN})}{V_{OUT} \times f_{SW} \times L \times 2} + I_{OUT}\frac{V_{OUT}}{V_{IN} \times \eta} \quad (6)$$

The inductor saturation current (I_{SAT}) should be greater than the maximum peak inductor current (I_{L_PEAK}).

2.6 Selecting the Input Capacitor

The converter has a discontinuous input current when it operates in buck and buck-boost mode, and requires a capacitor to supply AC current to the converter while maintaining the DC input voltage. For the best performance, use low-ESR capacitors. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients.

It is strongly recommended to use an another, lower-value capacitor (e.g. 0.1µF) with a small package size (e.g. 0603) to absorb high-frequency switching noise. Place the small-sized capacitor as close to PVIN and GND as possible. It is recommended to place two bypass capacitors close to the PVIN pins (pins 6 and 8) and VIN pin (pin 27), respectively. Since CIN absorbs the input switching current, it requires an adequate ripple current rating.

The RMS current in the input capacitor in buck mode can be estimated with Equation (7):

$$I_{CIN} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \quad (7)$$

The input voltage ripple should be less than 1% at the transition points. Excessive voltage ripple can cause EMI and hysteresis issues. Calculate ΔV_{IN} in buck-boost mode with Equation (8):

$$\Delta V_{IN} = ESR \left(\frac{I_{OUT} \times V_{OUT}}{V_{IN} \times \eta} + \frac{\Delta I_L}{2}\right) + \frac{I_{OUT} \times V_{OUT}}{V_{IN} \times \eta} D_{BUCK}(1 - D_{BUCK}) \quad (8)$$

2.7 Selecting the Output Capacitor

The converter also has a discontinuous output current in boost and buck-boost mode, and requires a capacitor to supply AC current to the load while maintaining the DC output voltage. Use ceramic, tantalum, or low-ESR electrolytic capacitors. The output capacitor's characteristics also affect the regulatory control system's stability. For the best results, use low-ESR capacitors to keep the output voltage ripple low. It is strongly recommended to use additional, lower-value capacitors (e.g. 0.1µF) with a small package size (0603) to absorb high-frequency switching noise. Place the small capacitors as close to the PVOUT and GND pins as possible.

The output voltage ripple should be less than 1% at the transition points. Excessive voltage ripple can cause EMI and hysteresis issues. Calculate ΔV_{OUT} in buck-boost mode with Equation (9):

$$\Delta V_{OUT} = ESR \left(\frac{I_{OUT} \times V_{OUT}}{V_{IN} \times \eta} + \frac{\Delta I_L}{2}\right) + I_{OUT} \frac{D_{BOOST}}{f_{SW} \times C_{OUT}} \quad (9)$$

3 MAXIMUM OUTPUT POWER

In general, the maximum output power is about 20W to 40W, and the power is constrained by electrical (current limit) and thermal parameters.

3.1 Thermal Constraints

The best method of determining the thermal constraints is measurement, with some margin for worst-case conditions. The worst-case V_{IN} may be the minimum voltage or minimum buck-boost voltage. A power loss estimation tool is also available for calculations (see Figure 5).

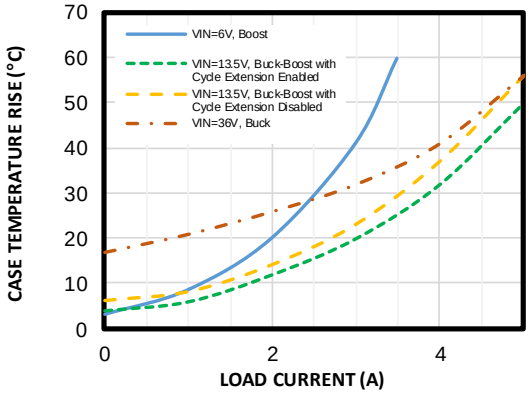

Figure 5: MPQ8875A Case Temperature Rise vs. Load Current

3.2 Current Limit

The MPQ8875A provides a peak/valley current limit scheme designed to limit the peak and valley inductor current to ensure that the switch currents remain within the device capabilities during overload or output short-circuit conditions. The maximum output power is limited by the current limit, especially in boost mode at a low V_{IN}. Calculate the peak inductor current with Equation (10):

$$I_{L\_PEAK} = \frac{V_{IN}(V_{OUT} - V_{IN})}{V_{OUT} \times f_{SW} \times L \times 2} + I_{OUT} \frac{V_{OUT}}{V_{IN} \times \eta} \quad (10)$$

For example, if V_{IN} = 6V, V_{OUT} = 12V, I_{RIPPLE} = 2A, efficiency = 95%, and the current limit = 9A, then the maximum output current can be determined as follows: (9A - 2A) x 0.95 x 6V / 12V = 3.33A (~40W). Alternately, if V_{IN} = 5V, V_{OUT} = 12V, I_{RIPPLE} = 2A, efficiency = 95%, and the current limit = 9A, then the maximum output current can be determined as follows: (9A - 2A) x 0.95 x 5V / 12V = 2.77A (~33W).

The exact minimum V_{IN} is critical for determining the maximum output power. Most applications also require knowing the maximum current limit.

4 KEY OTP DECISIONS

The MPQ8875A provides a one-time-programmable (OTP) memory for setting the custom default parameters. MPS provides a GUI and I²C to program the MPQ8875A during the development process. To program in application, contact MPS.

4.1 Setting the Output Voltage

Figure 6 shows the typical application circuit recommended for proper operation of the MPQ8875A.

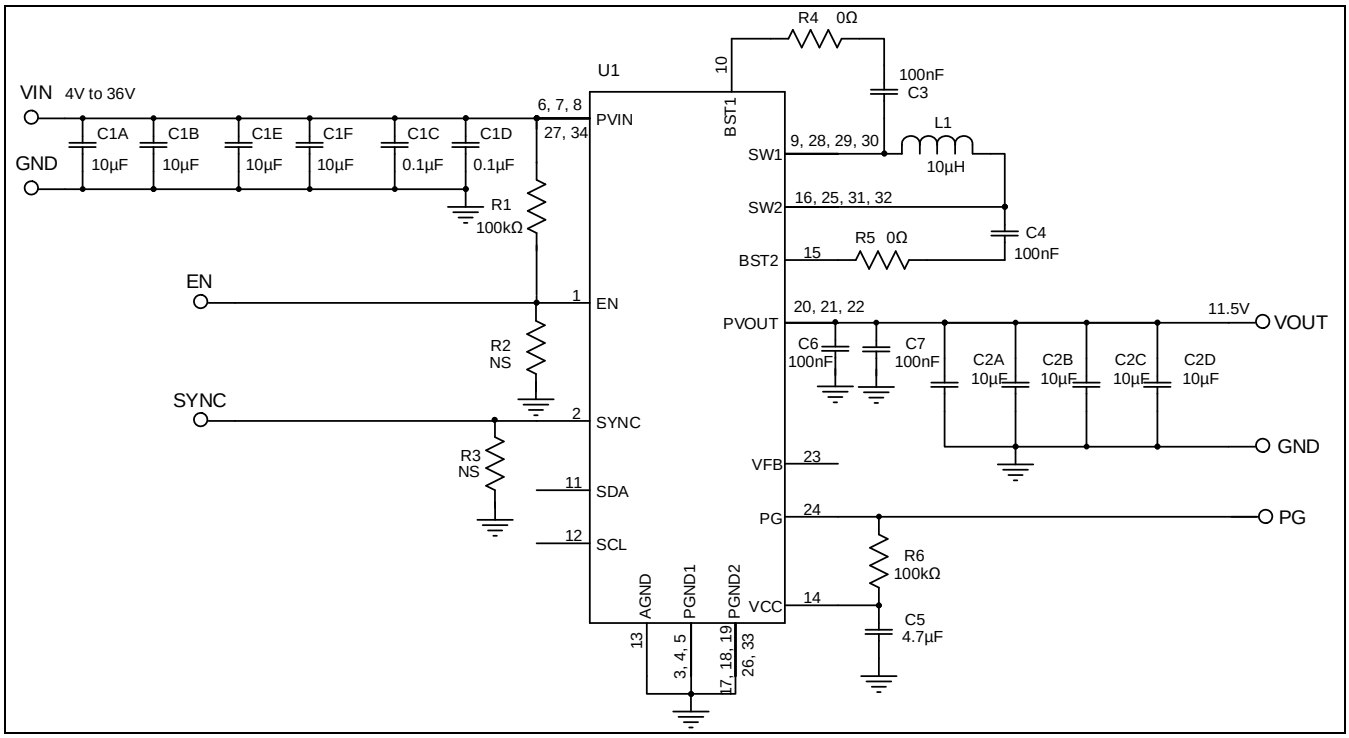

Figure 6: MPQ8875A Typical Application Circuit (V_{OUT} = 11.5V, f_{SW} = 450kHz)

OTP registers 00h and 01h set the output voltage.

Register 00h							
Bit 7 (R/W)	**Bit 6 (R/W)**	**Bit 5 (R/W)**	**Bit 4 (R/W)**	**Bit 3 (R/W)**	**Bit 2 (R/W)**	**Bit 1 (R/W)**	**Bit 0 (R/W)**
REF7	REF6	REF5	REF4	REF3	REF2	REF1	REF0
Bit Field Definitions							
Bits	**Field Name**	**Description**					
7:0	REF[7:0]	**Sets** the reference voltage. **V_{REF} = REF[7:0] x 10mV. The resolution is 10mV.** In low-input mode, REF7 is screened.					

<table>
<tr><th colspan="8">Register 01h</th></tr>
<tr><th>Bit 7 (R/W)</th><th>Bit 6 (R/W)</th><th>Bit 5 (R/W)</th><th>Bit 4 (R/W)</th><th>Bit 3 (R/W)</th><th>Bit 2 (R/W)</th><th>Bit 1 (R/W)</th><th>Bit 0 (R/W)</th></tr>
<tr><td>PWRCVTEN</td><td>INMD</td><td>RESERVED</td><td>DVSTEP1</td><td>DVSTEP0</td><td>FBDR2</td><td>FBDR1</td><td>FBDR0</td></tr>
<tr><th colspan="8">Bit Field Definitions</th></tr>
<tr><th>Bits</th><th colspan="2">Field Name</th><th colspan="5">Description</th></tr>
<tr><td>7</td><td colspan="2">PWRCVTEN</td><td colspan="5">Power converter on/off control.
0: Disabled
1: Enabled</td></tr>
<tr><td>6</td><td colspan="2">INMD</td><td colspan="5">Selects normal or low-input mode.
0: Normal input mode
1: Low-input mode</td></tr>
<tr><td>5</td><td colspan="2">RESERVED</td><td colspan="5">Reserved</td></tr>
<tr><td>4:3</td><td colspan="2">DVSTEP [1:0]</td><td colspan="5">Sets the time of each step in soft start and V_{OUT} dynamic adjustment mode (in µs).
00h 20 01h 41.67
02h 83.33 03h 166.67</td></tr>
<tr><td>2:0</td><td colspan="2">FBDR[2:0]</td><td colspan="5">Sets the V_{OUT} divider ratio.
00h 1 01h 1/2
02h 1/3 03h 1/5
04h 1/10 05h 1/20
06h/ 07h 1/30
For example, if FBDR[2:0] = 04h, then V_{FB} = 1 / 10 x V_{OUT}.</td></tr>
</table>

Write the EA reference voltage REF[7:0] to register 00h, and the divider ratio of FBDR[2:0] to register 01h. V_{OUT} can be calculated with Equation (11):

$$V_{OUT} = \frac{REF[7:0] \times 10mV}{FBDR[2:0]} \quad (11)$$

For example, if REF[7:0] = 73h, FBDR[2:0] = 04h, then V_{OUT} = 115 x 10mV / (1 / 10) = 11.5V.

Set the resistor divider and reference voltage. Note that most applications use a 1/10 resistor divider. The reference voltage (V_{REF}) can be changed during operation. DVSTEP changes the soft-start time.

4.2 Spread Spectrum

The MPQ8875A features frequency spread spectrum to further optimize EMI performance. The reference frequency, as well as the frequency spread spectrum modulation range and cycle, are all set via the I^2C interface. Once frequency spread spectrum is enabled, triangular frequency modulation mode is used to vary the switching frequency between the same ratio, both higher and lower than the reference value.

Throughout and entire modulation cycle, the switching frequency varies from the lowest to the highest, then drops back to the lowest. If an external clock signal is applied to the SYNC pin in synchronized input mode, the frequency spread spectrum mechanism is screened.

Using spread spectrum is recommended to ensure that the application passes EMC requirements. A good starting point for most applications is a 5% modulation range and 9000Hz modulation frequency.

Register 04h							
Bit 7 (R/W)	**Bit 6 (R/W)**	**Bit 5 (R/W)**	**Bit 4 (R/W)**	**Bit 3**	**Bit 2 (R/W)**	**Bit 1 (R/W)**	**Bit 0 (R/W)**
FSSEN	FSSMR2	FSSMR1	FSSMR0	RESERVED	FSSMC2	FSSMC1	FSSMC0

Bit Field Definitions

Bits	Field Name	Description
7	FSSEN	Enables frequency spread spectrum. 0: Disabled 1: Enabled
6:4	FSSMR[2:0]	Sets the frequency spread spectrum modulation range (in 1% of f_{SW}). 00h: ±3 | 01h: ±5 02h: ±10 | 03h: ±12.5 04h: ±20 | 05h: ±25 06h/07h: ±30 For example, if FSSMR[2:0] = 02h and f_{SW} = 2MHz, then the spread spectrum mode modulates the oscillator between 1.8MHz and 2.2MHz (±10% of f_{SW}).
3	RESERVED	Reserved.
2:0	FSSMC[2:0]	Sets the frequency spread spectrum modulation frequency (in Hz). 00h: 250 | 01h: 500 02h: 1000 | 03h: 2000 04h: 3000 | 05h: 4000 06h: 8000 | 07h: 9000

4.3 Compensation

The MPQ8875A integrates a high-performance operational amplifier to implement control loop compensation for stable output voltage regulation (see Figure 7). A SIMPLIS model is available to help set the compensation. Contact MPS for additional assistance in setting the compensation.

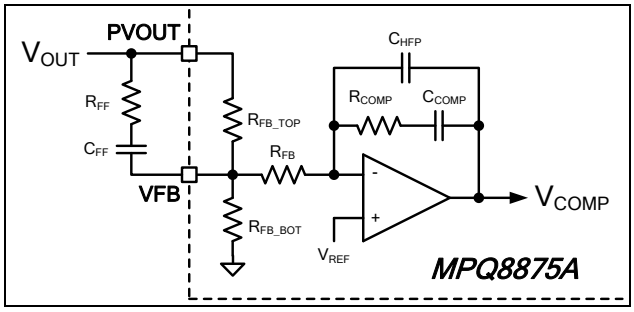

Figure 7: Compensation Network

The loop gain cannot be measured directly, but output impedance vs. frequency can show stability. The worst-case stability is maximum load and minimum V_{IN}.

Register 06h							
Bit 7 (R/W)	**Bit 6 (R/W)**	**Bit 5 (R/W)**	**Bit 4 (R/W)**	**Bit 3 (R/W)**	**Bit 2 (R/W)**	**Bit 1 (R/W)**	**Bit 0 (R/W)**
RFB2	RFB1	RFB0	RCOMP4	RCOMP3	RCOMP2	RCOMP1	RCOMP0

Bit Field Definitions

Bits	Field Name	Description
7:5	RFB[2:0]	Selects R_{FB}. R_{FB} = RFB[2:0] x 30kΩ + 50kΩ.
4:0	RCOMP[4:0]	Selects R_{COMP} (in kΩ).

00h	50	01h	173
02h	297	03h	420
04h	544	05h	667
06h	791	07h	914
08h	1038	09h	1161
0Ah	1284	0Bh	1408
0Ch	1531	0Dh	1655
0Eh	1778	0Fh	1902
10h	2025	11h	2148
12h	2272	13h	2395
14h	2519	15h	2642
16h	2766	17h	2889
18h	3012	19h	3136
1Ah	3259	1Bh	3383
1Ch	3506	1Dh	3630
1Eh	3753	1Fh	3877

Register 07h							
Bit 7 (R/W)	**Bit 6 (R/W)**	**Bit 5 (R/W)**	**Bit 4 (R/W)**	**Bit 3 (R/W)**	**Bit 2 (R/W)**	**Bit 1 (R/W)**	**Bit 0 (R/W)**
CHFP2	CHFP1	CHFP0	CCOMP4	CCOMP3	CCOMP2	CCOMP1	CCOMP0

Bit Field Definitions

Bits	Field Name	Description
7:5	CHFP[2:0]	Selects C_{HFP} (in pF).

00h	0.5	01h	1
02h	3	03h	5
04h	6	05h	8
06h	9	07h	10

4:0	CCOMP[4:0]	Selects C_{COMP}. 00h to 1Fh: C_{COMP} = (CCOMP[3:0] + 1) x 5pF. 5pF to 160pF.

5 CONCLUSION

The MPQ8875A's buck, boost, and buck-boost performance can be optimized with various technical methods. This application note proposed a method to optimize the MPQ8875A's circuit design. A design example was provided, as well as test results and registers map to demonstrate the validity of buck-boost optimized operation.

6 ADDITIONAL READING

For more information about automotive MPS buck-boost products, contact your MPS FAE or visit the MPS website at:

https://www.monolithicpower.com/en/applications/automotive.html