Motor Driver PCB Layout Guidelines

Application Note

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ABSTRACT

Motor driver ICs are able to deliver large amounts of current and dissipate a significant amount of power primarily due to the I^2R power dissipated in the $R_{DS(ON)}$ of the internal MOSFETs. Generally, this power is dissipated into copper areas on the printed circuit board (PCB). To ensure adequate cooling, special PCB design techniques are required. This application note describes some techniques used to complete good PCB designs using these ICs.

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INTRODUCTION

Printed circuit board (PCB designs for motor driver ICs require some techniques not required in normal analog and digital circuits. This application note describes the types of IC packages commonly used for motor driver ICs and provides specific recommendations for designing PC boards that use them.

MOTOR DRIVER PACKAGES

There are a number of different IC packages used for motor driver ICs. At Monolithic Power Systems (MPS), four basic groups of packages are used: SOT23 and SOIC packages, TSSOP packages, QFN packages, and flip-chip QFN packages.

SOIC and SOT23 Packages

SOT23 packages are small packages originally designed to house discrete devices like transistors. The SOIC package is a standard IC package. Examples of these packages are shown in Figure 1 below.

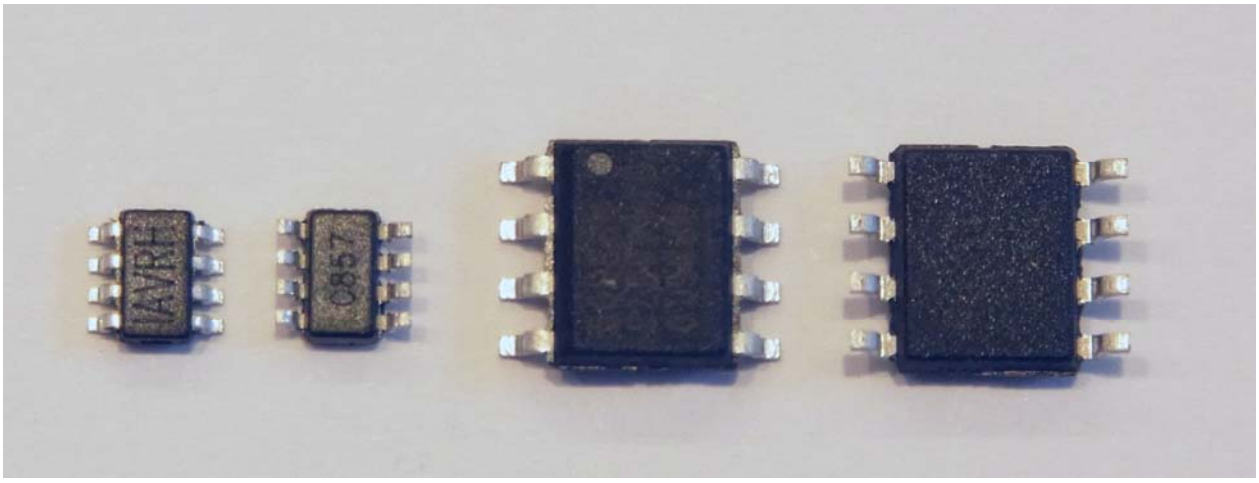

Figure 1: SOT23 and SOIC Packages

Often, to maximize the power dissipation capability of these leaded packages, MPS uses a “flip-chip on leadframe” construction (see Figure 2). The silicon die is bonded to the metal leads using copper bumps and solder without the use of bond wires. This allows heat to be conducted from the die through the leads to the PCB.

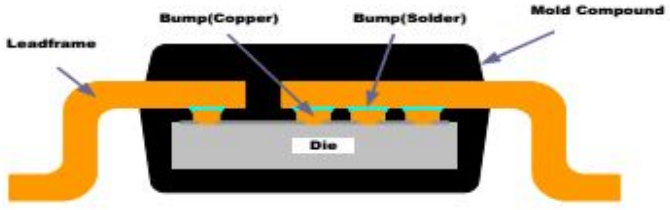

Figure 2: Flip Chip on Leadframe Structure

TSSOP Packages

TSSOP packages are rectangular in shape and use two rows of pins. The pins are connected to the die using wires bonded between the chip and the lead frame, so not much heat is conducted through the leads. TSSOP packages used for motor driver ICs usually have a large exposed pad on the underside of the package that helps remove heat from the device (see Figure 3).

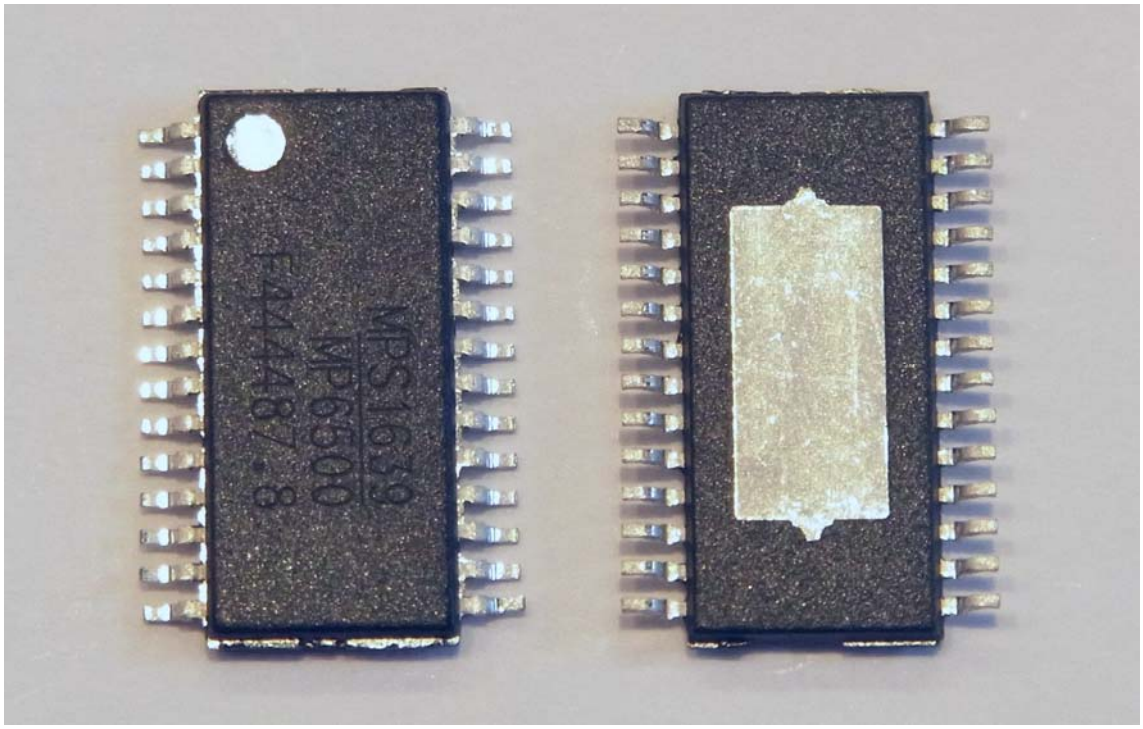

Figure 3: TSSOP Package

To remove heat from this type of package, a well-soldered connection must be made to the exposed pad. This pad is normally at ground potential, so it can be tied into the PCB ground plane.

QFN Packages

QFN packages are leadless packages that have pads around the outside edges of the part, as well as a larger pad centered on the underside of the device (see Figure 4). This larger pad is used to extract heat from the die. The pads along the periphery are connected to the die using wires bonded between the chip and the lead frame.

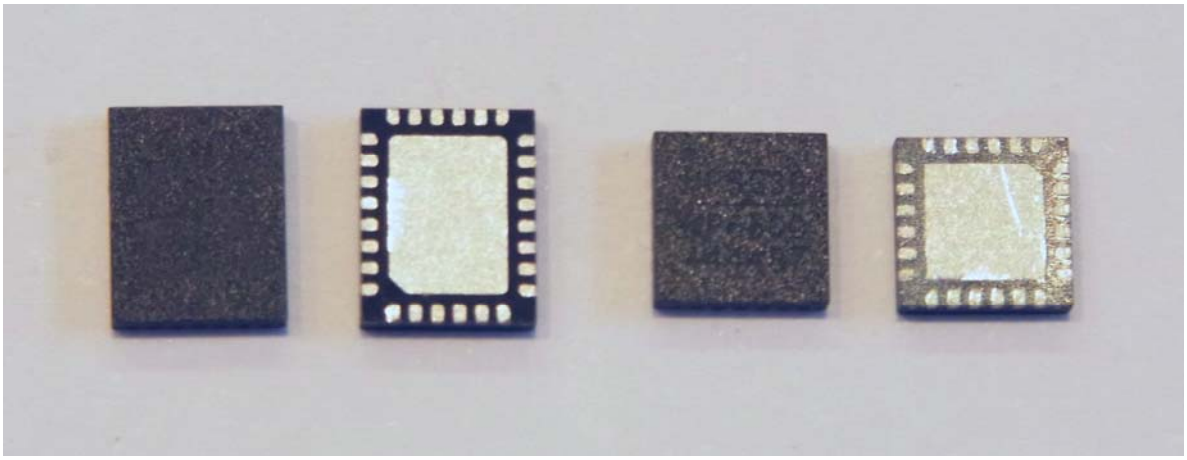

Figure 4: QFN Packages

Like in the TSSOP package, the exposed pad in the center of the QFN package must be soldered to the PCB to provide a path for heat to be dissipated.

Flip-Chip QFN Packages

MPS' exclusive FCQFN packages are similar to regular QFN packages, but instead of using wire bonds to connect the die to the package pads, the die is flipped upside-down and directly connected to the pads on the underside of the device. The pads can be placed directly opposite the heat-generating power devices on the die, so they are often arranged as long stripes instead of small pads (see Figure 5).

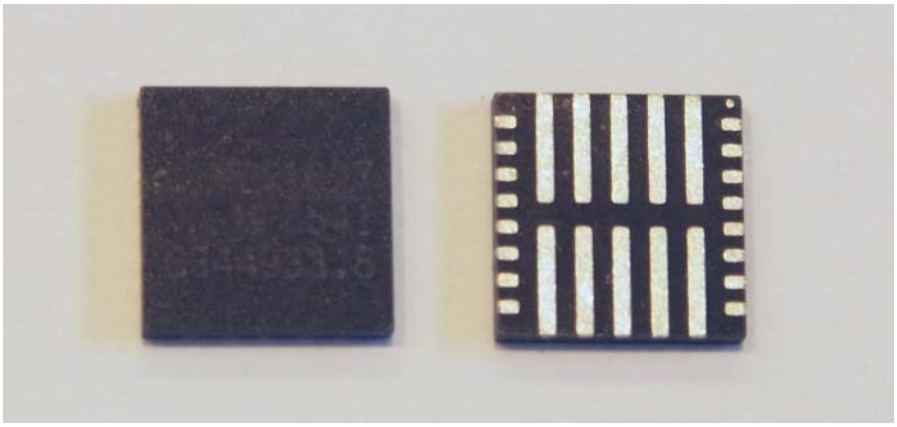

Figure 5: Flip-Chip QFN Package

These packages use rows of copper bumps on the surface of the die, which are then bonded to the leadframe with solder (see Figure 6 and Figure 7).

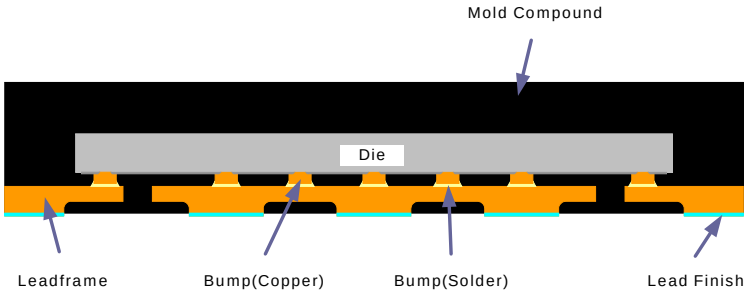

Figure 6: FCQFN Structure

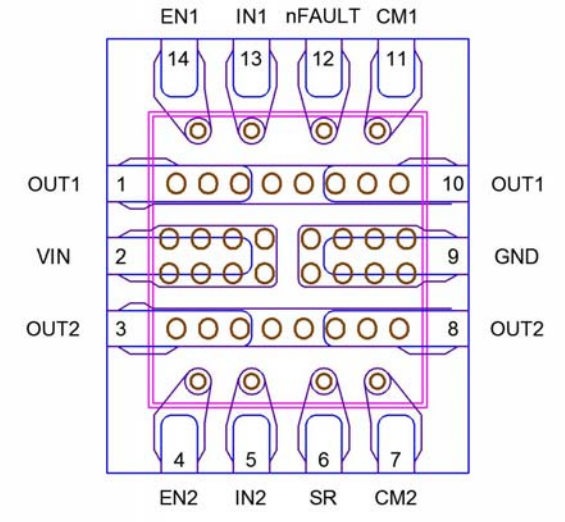

Figure 7: Copper Bump Layout

GENERAL PCB DESIGN TECHNIQUES

Copper Area

Copper is an excellent heat conductor. PCB substrate material, such as FR-4 glass epoxy, is a poor heat conductor. Therefore, from a thermal management perspective, the more copper area on a PCB, the better.

Thick copper, such as 2-ounce foil (68 microns), conducts heat better than thinner copper. Unfortunately, thick copper is quite expensive and difficult to achieve fine geometries with. Generally, 1-ounce (34 microns) copper is standard, especially for devices with a 0.5mm pin pitch or smaller. For external layers, ½-ounce copper plated up to 1-ounce thickness is used.

Solid copper planes used on the inner layers of multi-layer boards spread heat well. However, since these planes are normally placed in the center of the board stack-up, the heat can be trapped inside the board. Adding copper areas on the outer layers of the PCB and placing many vias to connect, or stitch, these areas to the inner planes helps transfer heat out of the planes.

On two-layer PCBs, spreading heat can be more difficult due to the presence of traces and components. Providing as much solid copper as possible with good thermal connections to the motor driver IC is a necessity. Putting copper pours on both outer layers and stitching them together with many vias helps spread heat across areas cut by traces and components.

Trace Width

Since the current in and out of a motor driver IC is large (exceeding 10A in some cases), the width of the PCB traces in and out of the device must be properly sized. The wider a trace is, the lower resistance it has. Traces must be sized so that there is no excessive power dissipated in the trace resistance, which would cause the trace to heat to unacceptable temperatures.

A common standard that designers use to determine trace width is the IPC-2221[1]. This specification has charts that show the necessary copper cross-sectional area for various current levels and allowable temperature rise (see Figure 8). This area can be converted to a trace width at a given copper layer thickness. For example, a trace carrying 10A of current in a 1-ounce copper layer needs to be just over 7mm wide to achieve a temperature rise of 10°C. At a 1A current, the width only needs to be 0.3mm.

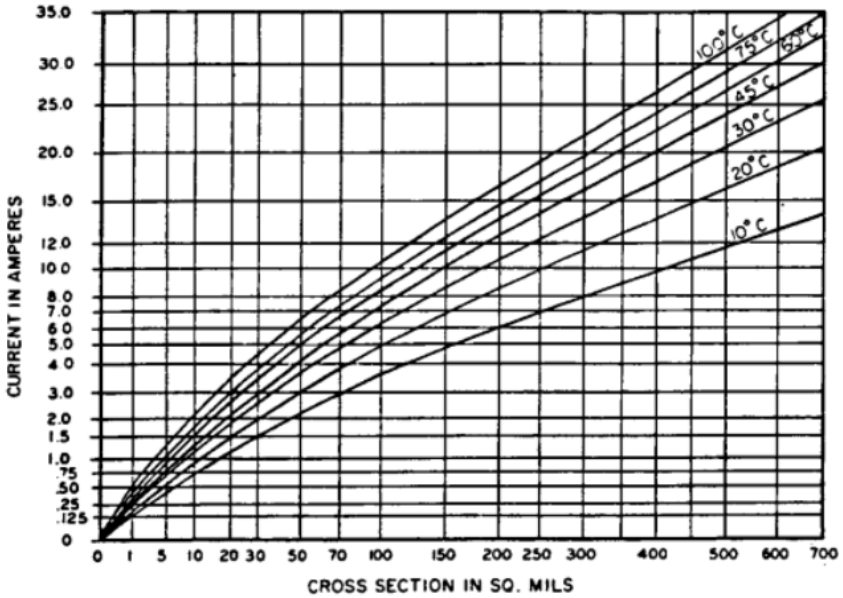

Figure 8: IPC-2221 Trace Cross-Sectional Area Chart

[1] IPC, "Generic Standard on Printed Circuit Board Design," IPC-2221.

Given this, it may seem impossible to run 10A of current through an IC pad that is less than 1mm in width.

It is important to understand that the trace width recommendations in the IPC-2221 apply to a long PCB trace of constant width. It is possible to pass much larger currents through a short section of PCB trace with no ill effects if they are connected to a larger trace or copper area. This is because the resistance of the short, narrow PCB trace is small, and any heat generated there is drawn into wider copper areas, which act as a heat sink.

As an example, refer to Figure 9. Even though the pads for this device (MP6515) are only 0.4mm wide, they must carry up to 3A of continuous current. To minimize any trace resistance problems, the trace is widened into as large a width as practical and as close to the device as possible.

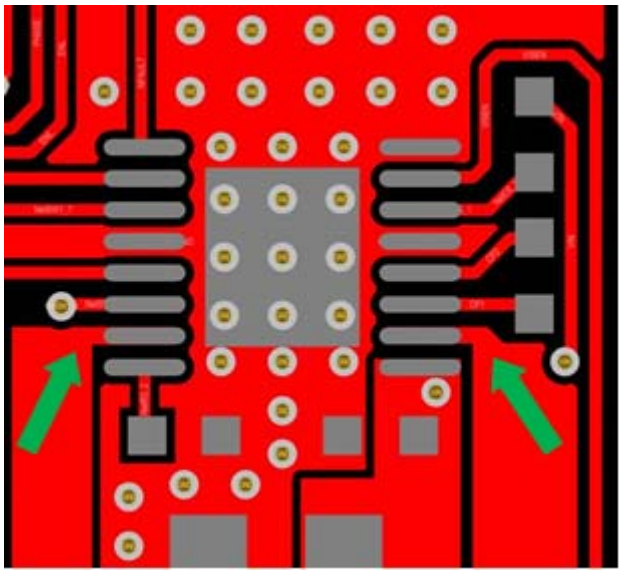

Figure 9: PCB Trade Widening

Any heat that is generated in the narrow portion of the trace is conducted to the wider copper areas, so the temperature rise in the narrow trace is negligible.

Traces embedded in the PCB's inner layers cannot dissipate heat as well as traces on the outer layers because the insulating substrate does not conduct heat well. For this reason, for a given current, the inner layer traces should be designed to be about twice as wide as those on the outer layers.

As a rough guideline, Table 1 shows the recommended trace widths for long (>~2cm) traces in motor driver applications.

Table 1: PCB Trace Widths

Current (RMS or DC)	Trace Width in 1oz Copper		Trace Width in 2oz Copper	
	Outer Layer	Inner Layer	Outer Layer	Inner Layer
≤1A	0.6mm	1.2mm	0.3mm	0.6mm
2.5A	1mm	2mm	0.5mm	1mm
5A	2.5mm	5mm	1.2mm	2.5mm
10A	7mm	14mm	3.5mm	7mm

If space permits, routing using even wider traces or copper pours minimizes temperature rise and voltage drop.

Thermal Vias

Vias are small plated holes that are typically used to transport a signal trace from one layer to another. Thermal vias are similar but are used to transmit heat from one layer to another. The proper use of thermal vias is critical to heat dissipation on a PCB, but there are several manufacturability issues that must be considered[2].

Vias have thermal resistance, which is some drop in temperature as heat flows through them. To minimize this resistance and make the via more effective at transmitting heat, the via should be large with as much copper area inside the hole as possible (see Figure 10).

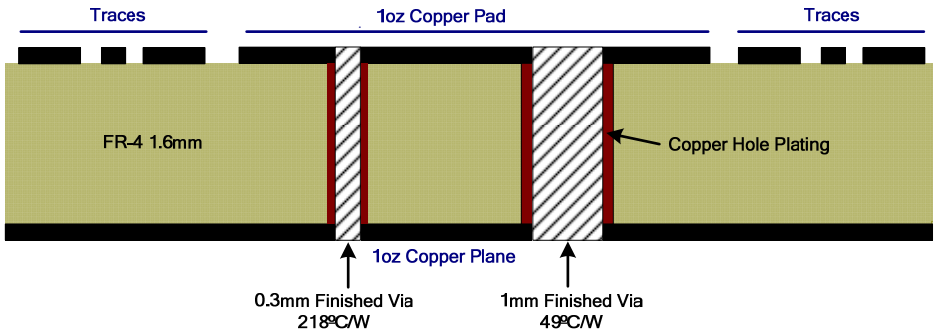

Figure 10: Via Cross-Section

Although using large vias in open areas of the PCB is possible, vias are often used within a pad area to move heat directly from the IC package. In this case, large vias cannot be used because a large plated hole would cause “solder wicking,” where the solder intended to connect the IC to the PCB flows down into the via, causing a poor solder joint.

There are several methods to reduce solder wicking. One is to use very small via holes so that the volume of solder wicked into the holes is minimal. However, small vias have more thermal resistance, so more are needed to achieve the same thermal performance.

Another method is to “tent” the vias on the backside of the board. This involves removing the opening in the solder mask on the back side so that the solder mask material covers the via. If the via hole is small, the solder mask will plug the via so solder cannot wick through the PCB. Unfortunately, this can cause flux entrapment.

With a plugged via, flux (which is a component of solder paste) can get trapped inside the via hole. Some flux formulations can be corrosive and result in reliability issues over time if they are not removed. Luckily, most modern “no-clean” flux processes are non-corrosive and will not cause a problem.

Note that thermal vias should never have “thermal reliefs.” They must be connected directly to the copper areas (see Figure 11).

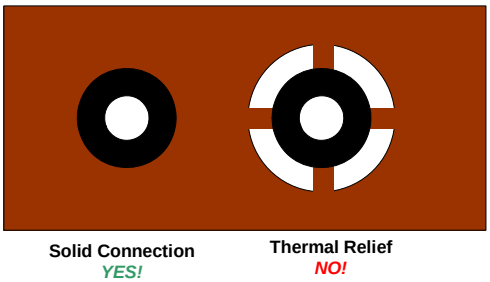

Figure 11: Thermal Reliefs

[2] IPC, “Design Guide for Protection of Printed Board Via Structures,” IPC-4761.

It is recommended that the PCB designer check with the SMT process engineers at the PCB assembler to choose the best via hole size and construction for that assembler's process, especially when thermal vias are placed within pad areas.

Soldering Exposed Pads

TSSOP and QFN packages have a large exposed pad underneath the part. This pad is connected to the backside of the die and used to remove heat from the device. It is imperative that this pad be well-soldered to an area of the PCB to dissipate power.

The corresponding MPS datasheet has a drawing that specifies the size of the copper pad that should be used on the PCB for the exposed pad.

The opening in the stencil used to deposit solder paste for this pad is not specified by MPS. Often, SMT process engineers have their own rules and preferences about how much solder should be deposited and what sort of pattern should be used on the stencil.

If a single opening similar in size to the pad is used, a large amount of solder paste is deposited. This can cause the device to be lifted up due to the surface tension of the solder when it melts. Another concern is "solder voiding," which is cavities or gaps inside areas of solder. Solder voiding can occur when the volatile component of flux vaporizes, or boils, during the solder reflow process. This can cause solder to be pushed out of the joint.

To address these issues, for pads that are more than about 2mm square, the paste is normally deposited in several small square or circular areas (see Figure 12). Dividing the paste into smaller areas allows the volatile flux components to more easily escape the paste without displacing the solder.

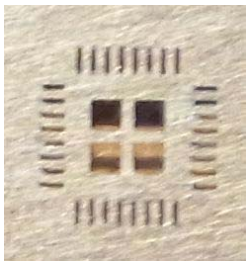

Figure 12: QFN Solder Stencil

MPS recommends that the PCB designer consult with SMT process engineers at the PCB assembler to design the correct stencil openings for these pads. There are also a number of papers available online that can help[3] [4] [5].

Component Placement

Component placement guidelines for motor driver ICs are similar to those of other types of ICs. Bypass capacitors should be placed as close to the device power pins as possible with bulk capacitors located nearby. Many motor driver ICs use bootstrap and/or charge pump capacitors, which should also be placed near the IC.

Refer to Figure 13 for an example of good component placement (the example shows a MP6600 stepper motor driver on a 2-layer PCB). Most signals are routed directly on the top layer. Power is routed from the bulk capacitors to the bypass and charge pump capacitors on the bottom layer, using multiple vias at the points where it changes layers.

[3] IPC, "Stencil Design Guidelines," IPC-7525.
[4] IPC, "Design and Assembly Process for Bottom Termination Components," IPC-7093.
[5] Ahmer Syed and WonJoon Kang, Amkor Technology, "Assembly and Reliability Considerations for QFN Type Packages."

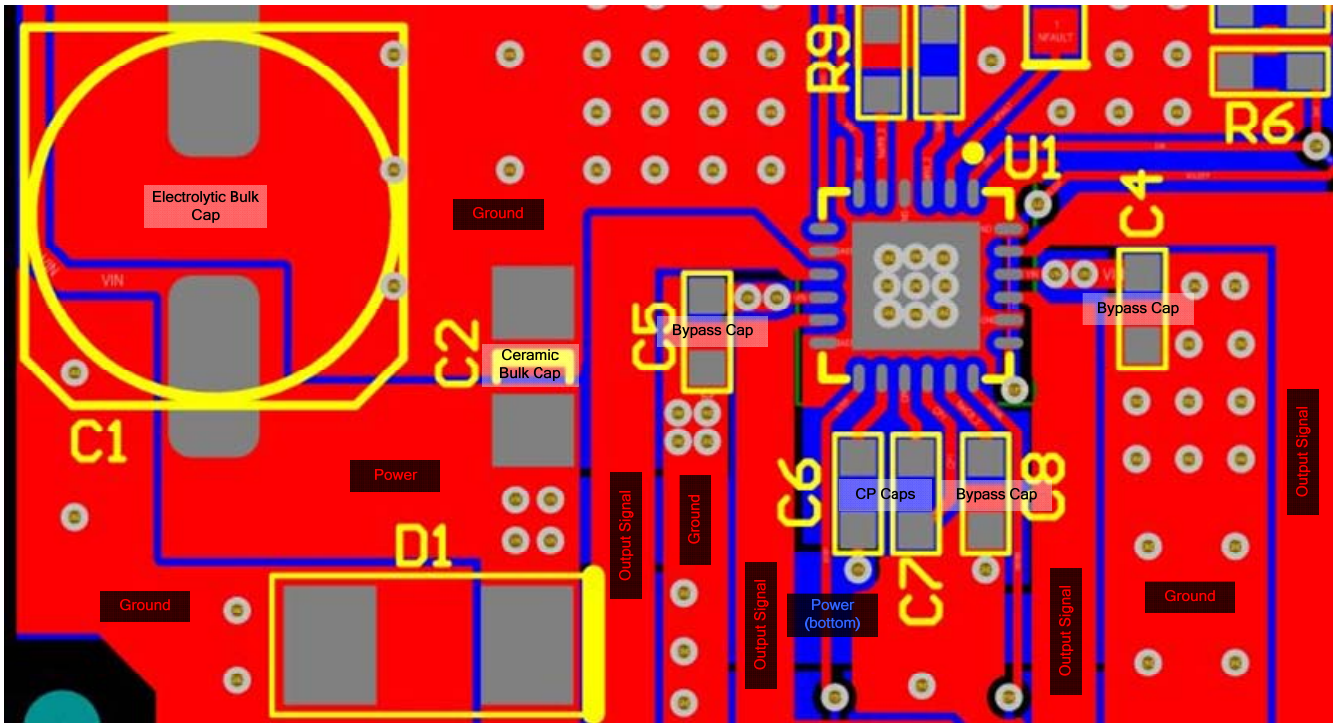

Figure 13: MP6600 Component Placement

SPECIFIC PCB DESIGN RECOMMENDATIONS

SOT23 and SOIC Packages

SOT23 and SOIC packages do not have a dedicated large pad for drawing heat from the device. Instead, heat is removed through the leads. To maximize thermal performance, large copper areas should be attached to the leads that carry high current. On a motor driver IC, typically the power, ground, and output pins should be attached to copper areas.

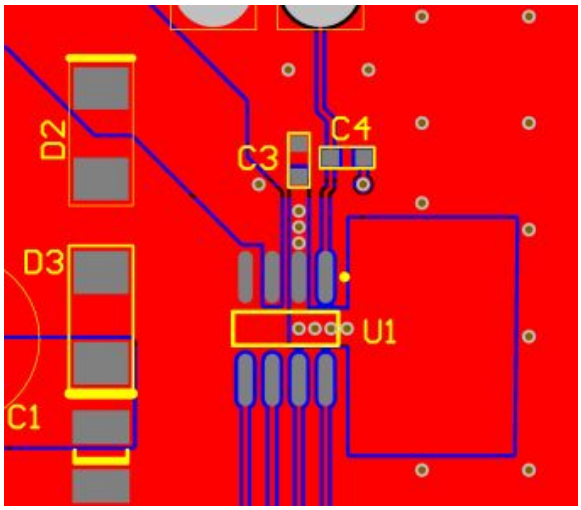

Figure 14: SOIC PCB Layout

Figure 14 shows a typical PCB layout for a flip-chip on a leadframe SOIC package, the MPQ6610 in this example. Pin 2 is the device power pin. A copper area is placed near the device on the top layer, and several thermal vias connect this area to copper on the back side of the PCB. Pin 4 is the ground and is connected to the copper ground pour on the top layer. Pin 3 is the device output, which is routed to a large copper area as well.

Note that there are no thermal reliefs on the SMT pads. They are solidly connected to the copper areas. This is critical for good thermal performance.

Since vias are not placed within pad areas, the vias can be made relatively large to provide lower thermal resistance.

QFN and TSSOP Packages

These packages have a large exposed pad that is bonded to the bottom of the die. Heat is conducted through the die to this pad and then through a soldered connection to copper on the PCB. Normally, an array of thermal vias is used to conduct the heat away from the device into large copper areas of the PCB, often a ground plane.

Ideally, thermal vias are placed directly in the pad area where the exposed pad is soldered to the PCB. The example in Figure 15 shows the MP6500 in a 28-pin TSSOP package with an array of 18 vias with a finished hole diameter of 0.38mm. This via array has a calculated thermal resistance of about 7.7°C/W.

Normally, finished hole sizes of 0.4mm and smaller are used for these thermal vias to prevent solder wicking. If smaller holes are required by the SMT process, more holes should be used to keep the overall thermal resistance as low as possible.

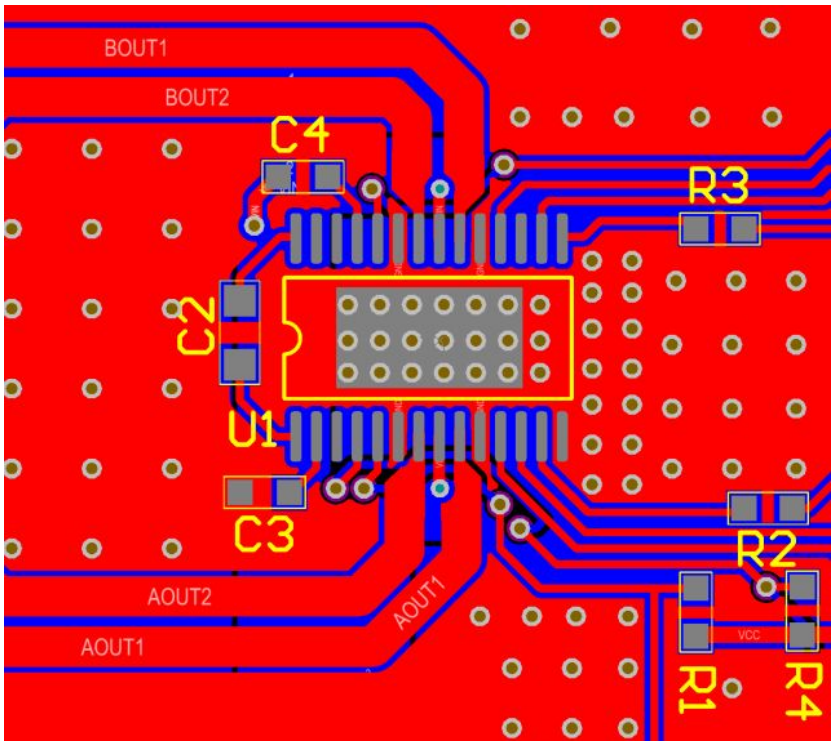

Figure 15: TSSOP PCB Layout

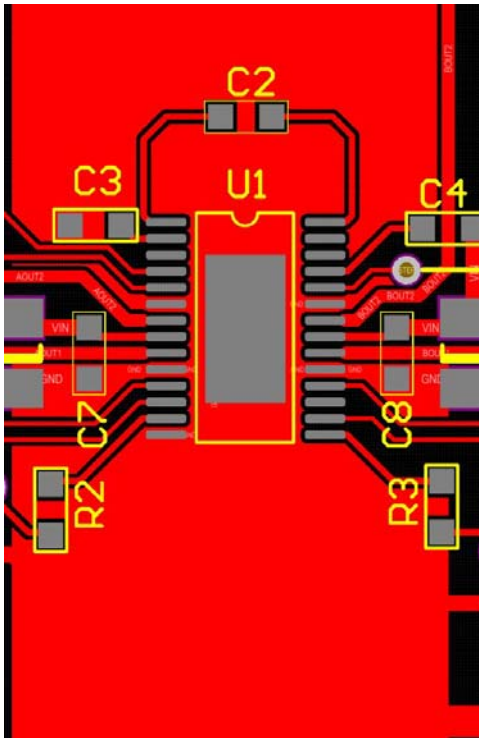

Figure 16: Single-Layer TSSOP Layout

In addition to the vias placed within the pad area, thermal vias are also placed in areas outside the IC body. In TSSOP packages where copper areas can extend beyond the ends of the package, this provides another path for heat to pass from the device through the top copper layer and out to other layers.

Copper can be used to remove heat from a TSSOP package, even in a single layer PCB design. In the example in Figure 16, using the same device used in Figure 15, copper extends from underneath the IC on the top layer in both directions, and no vias are used. Note that the placement of C2 cuts off much of the thermal path on that end of the IC, so it is placed away from the IC to allow for at least some copper area to dissipate heat at that end of the device.

With QFN devices, there are pads on all four edges of the package that prevent the use of copper in the top layer to extract heat. The use of thermal vias is mandatory to pull heat out to either an inner plane or the bottom layer of the PCB.

The PCB layout in Figure 17 shows a small 4mmx4mm QFN device, the MP6600. Only nine thermal vias fit in the exposed pad area. Because of this, the thermal performance of this PCB is not as good as the TSSOP package shown above. Consequently, this device drives less current than the same part in a TSSOP package.

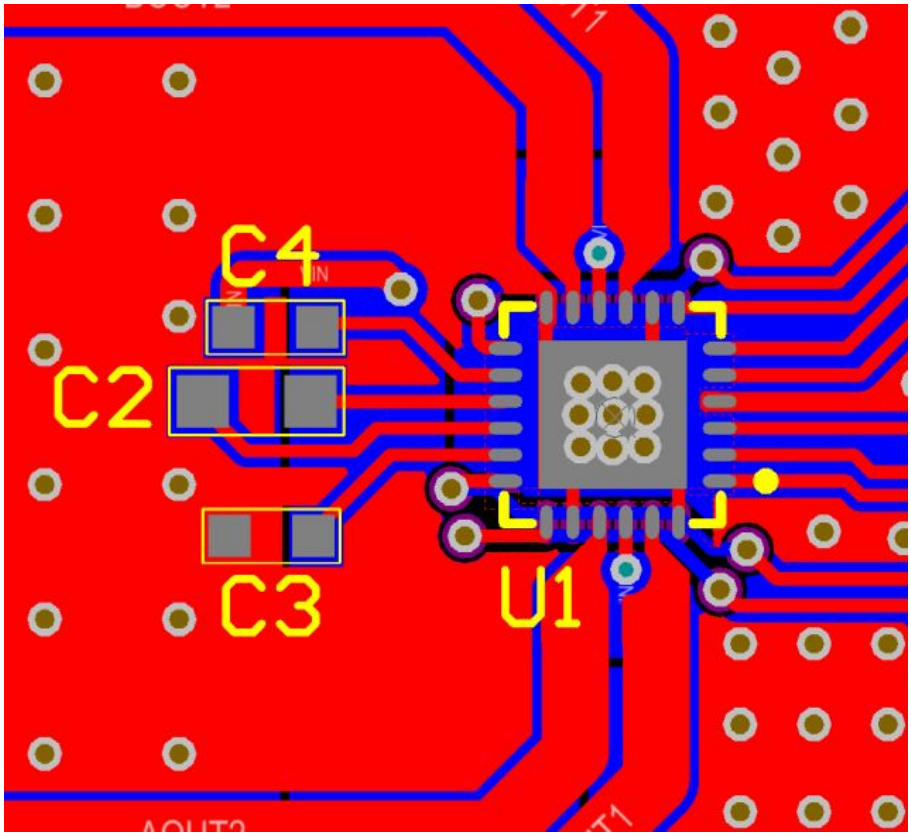

Figure 17: 4mmx4mm QFN Layout

Flip-Chip QFN Packages

Flip-chip QFN (FCQFN) packages often have irregularly shaped pads, or pads arranged in long, narrow stripes. Unlike normal QFN packages, heat is extracted through many of these pads instead of one large central pad. This creates a bit of a challenge for the PCB design, since there are many pads, all carrying different signals, that need to be connected to copper areas.

In some cases, small vias can be placed within these pad areas, similar to what is done with regular QFN packages. On multilayer boards with power and ground planes, vias can be connected from these pads directly to the planes. In other cases, copper must be attached directly to the pads to draw the heat away from the IC into larger copper areas.

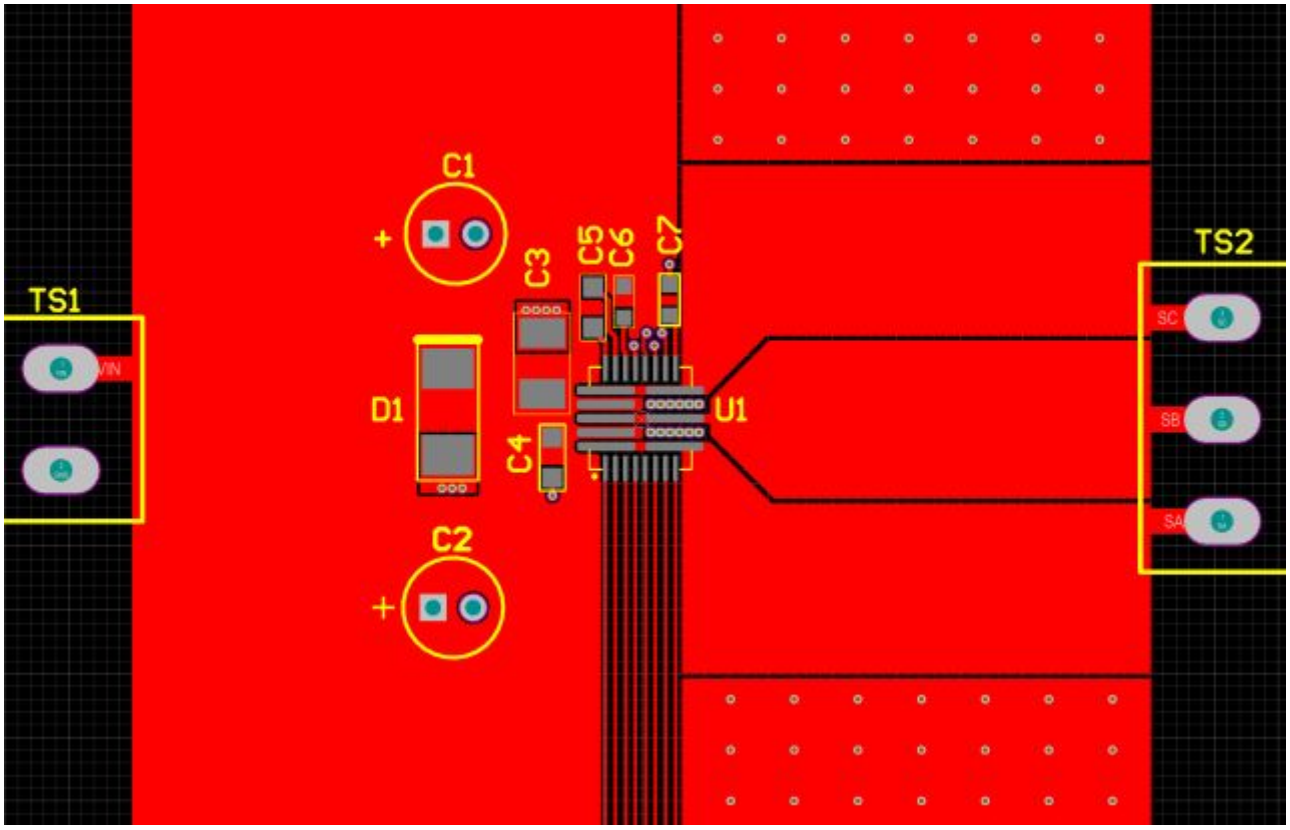

Figure 18: FCQFN PCB Layout

Figure 8 shows a PCB layout for a MP6540 power stage. This device has long pads for power, ground, and the three outputs. Note that the MP6540 package is only 4mmx4mm.

The copper area to the left of the device is the power input. This large copper area is directly connected to the two power pads of the device.

The three output pads are connected to copper areas to the right of the device. Note how the copper area is expanded as much as possible just after exiting the pad. This provides good heat transfer from the pad to the ambient air.

Notice the row of small vias within two of the pads at the right side of the device. These pads are connected to ground, and a solid ground plane is placed on the back side of the PCB. These vias are 0.46mm in diameter, with a finished drill hole of 0.25mm. The vias are small enough to fit within the pad area and not violate the PCB spacing rule (which requires 6mils, or 0.15mm, clearance). Use as many vias as will fit within the pad area (in this case, six per pad).

If the SMT process forbids the placement of vias within the pad structure, then often the only option is to route out of the pad to connect to vias, as shown in Figure 19. This results in poorer thermal performance than placing vias directly in the pads, but it does remove any concern of solder wicking into the holes.

A thermal image taken of the MP6540 driving 4A of current into a BLDC motor shows the heat being extracted from the device into the copper areas (see Figure 20). This example uses a two-layer PCB 4cmx4cm in size using standard one-ounce copper, 1.6mm thick FR-4 PCB material, and the layout shown in Figure 18.

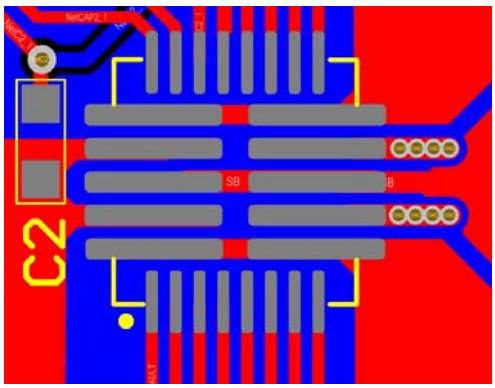

Figure 19: Vias Outside Pads

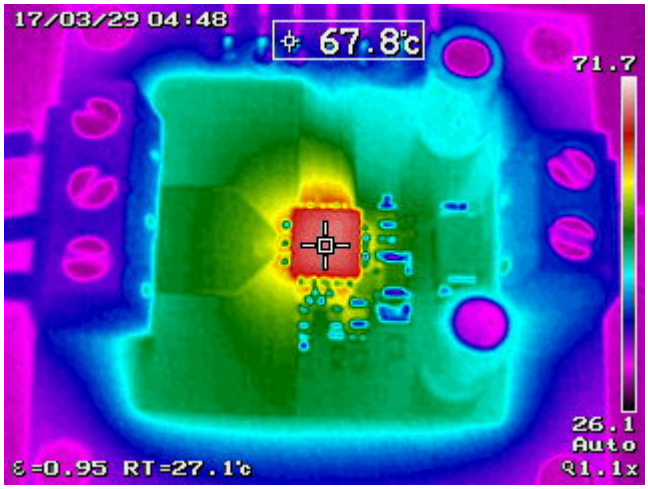

Figure 20: MP65640 Thermal Image

The solder stencil design for the type of package shown in Figure 21 is similar to normal IC packages with small leads. The stencil openings are sized about the same as the pads. Again, it is recommended that the PCB assembler's SMT process engineers be consulted on the stencil design.

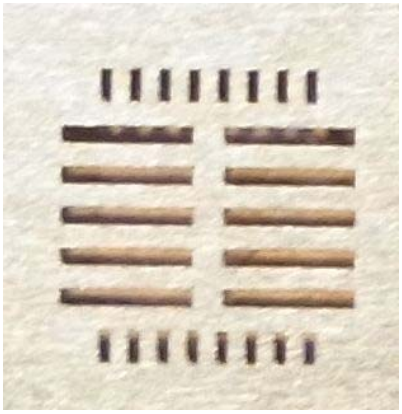

Figure 21: FCQFN Stencil